AFIT/GE/ENG/93D-33

The AFIT Multielectrode Array for Neural Recording and Stimulation: Design, Testing, and Encapsulation

THESIS

James R. Reid Jr.
Second Lieutenant, USAF

AFIT/GE/ENG/93D-33

AFIT/GE/ENG/93D-33

The AFIT Multielectrode Array for Neural Recording and Stimulation: Design, Testing, and Encapsulation

THESIS

Presented to the Faculty of the Graduate School of Engineering
of the Air Force Institute of Technology
Air University
In Partial Fulfillment of the
Requirements for the Degree of
Master of Science in Electrical Engineering

James R. Reid Jr., B.S.E. E.
Second Lieutenant, USAF

December, 1993

Acknowledgements

I would first like to thank my committee members, Dr. Steven K. Rogers, Dr. Victor M. Bright, and Dr. Matthew Kabrisky, for providing the inspiration and support needed to do this thesis. It was only through their encouragement and suggestions that it was possible to complete this thesis.

Special thanks goes Bill Trop and Chris O'Brien of the AFIT Cooperative Electronics, Materials, and Processes Laboratory, for keeping the "one of a kind" machines running. But mostly thanks for making sure the burgers were cooked well at the monthly bar-B-Qs!

James R. Reid Jr.

Table of Contents

List of Figures

List of Tables

Abstract

A two-dimensional, X-Y addressable, multiplexed array of 256 electrodes (16 x 16) has been fabricated using conventional semiconductor processing techniques. The individual electrodes are $160\mu m \times 160\mu m$, approximating the size of the cortical columns; the overall array size is $3910\mu m \times 3910\mu m$. The array has been fitted to a chronically implantable package and tested for several days in a simulated neural environment. EEG-like data were collected successfully from individual electrodes in the array. This array improves on a previous design of a 16 electrode (4 x 4) array that was chronically implanted on the cortex of a laboratory beagle (Canis familiaris) in 1982. The original implant, located approximately over primary visual cortex, recorded both EEG and visually evoked response (VER) data. It proved the feasibility of multiplexing data directly from the surface of the cortex, thereby opening the possibility of very large arrays of electrodes since only a single wideband signal channel could address significant numbers of electrodes.

The AFIT Multielectrode Array for Neural Recording and Stimulation: Design, Testing, and Encapsulation

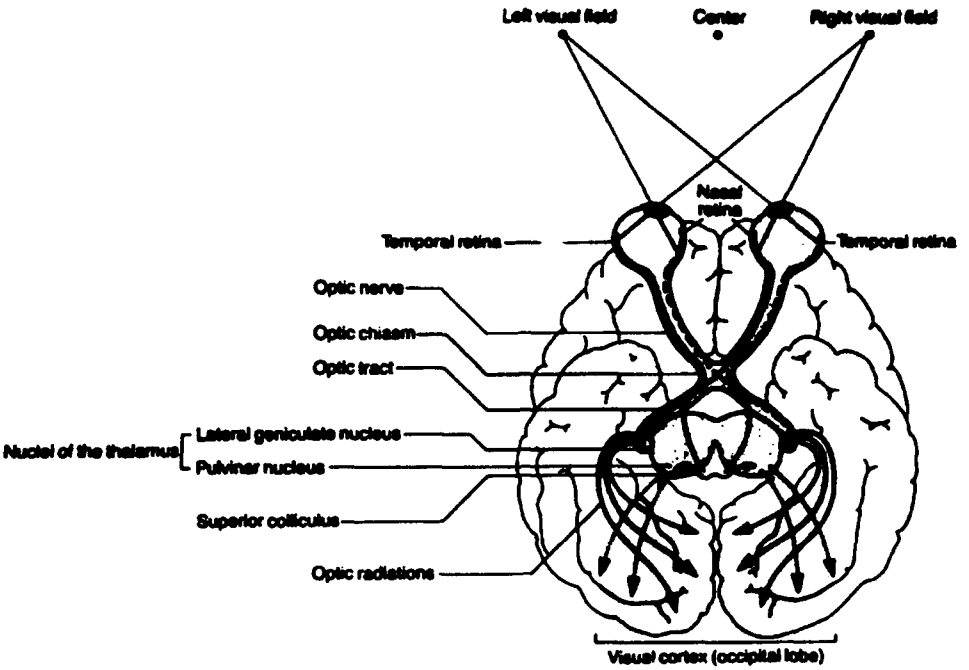
I. Introduction

1.1 Background

Scientists have been working for years to build machines capable of recognizing complex images. However, tasks such as recognizing a familiar face or reading a book have proven very difficult to perform with machines. Humans, on the other hand, perform these tasks with minimal conscious effort. Some scientists have, therefore, worked to understand the human visual system, with the hope that they will learn enough to build machines capable of recognizing complex objects.

Past research on the brain has produced a general mapping of the brain's visual data pathways. Neural pathways beginning in the retina, going to the lateral geniculate nucleus, and then to visual area one (V1) of the neocortex, have been mapped in detail (10). This includes a mapping of the visual field onto the area V1 (29). It is also known that extensive connections exist from V1 to several other areas of the brain, particularly, visual areas two through five (V2-V5). V1 through V5 are located at the back of the brain in an area generally referred to as the visual cortex (5). Figure 1.1 shows a general map of the human visual system.

The detailed information about the front end of the visual system, from the eyes to V1, has not unlocked the brain's secrets for recognizing objects. Therefore, scientists have been trying to study the function and interconnection of the back end of the visual system, or V1 through V5. It is believed that these areas perform the higher level tasks necessary for image recognition.



Excerpted from The Computational Brain (5:151).

Figure 1. Pathways of the human visual system.

Efforts to study areas V1 through V5 have focused around two methods: electroencephalographs or EEGs, and micro-probe electrodes (1, 12, 15, 16, 17, 25). EEGs are measured by placing electrodes on or in the scalp of a subject. These electrodes record electric potentials at a gross level. From EEGs, scientists are able to tell what part of the brain is most active at a given time. Therefore, EEGs are capable of telling scientists which part of the brain should be studied in greater detail for them to understand a given process. For instance, when an image is presented to a subject, EEGs show a peak of activity occurring in the visual cortex approximately 100 milliseconds after the image is presented. Further, a second peak will occur at approximately 300 milliseconds (25). This peak is believed to be when the brain recognizes the image. Unfortunately, this tells very little about how the brain functions.

At the other extreme, micro-probe electrodes allow scientists to study the function of individual neurons in the brain. Therefore, scientists can learn detailed

information about how a specific neuron responds to incoming signals. By looking at several neurons in one area of the brain, scientists are able to learn some details about how that isolated area of the brain functions. However, these electrodes can only be used a few at a time. Further, they typically require that the subject be sedated. Therefore, the brain is observed in non-typical operation, and the function of the neurons may differ from normal. It is thus difficult to gain an understanding of interconnections in the brain.

To further understand the brain, scientists need a method to study the brain at a level between the coarse resolution of the EEG and the fine resolution of the micro-probe electrodes.

Several scientists (6, 15, 19) have suggested that the neocortex is grouped into cortical columns. Cortical columns contain several hundred to several thousand neurons that function together to perform specific tasks. Kabrisky has further suggested, that an analysis of the interconnection matrix between these cortical columns may provide new insight to the function of the brain (20). Currently, no device has been successfully fabricated to study the brain at this level.

1.2 Problem Statement

Here at the Air Force Institute of Technology (AFIT), a semiconductor array to study the brain at the level of the cortical column has been under development (3, 9, 13, 24, 26, 28, 30). However, a successful implantation package incorporating this design has not been fabricated. Therefore, this thesis is aimed at fabricating an implantable array package. This work consists of three major areas. First, previous design errors in the array's circuitry must be corrected. Second, a method for protecting the array from the environment it will be exposed to during implantation must be developed. And third, a package suitable for implantation must be developed to connect the device to the external electronics.

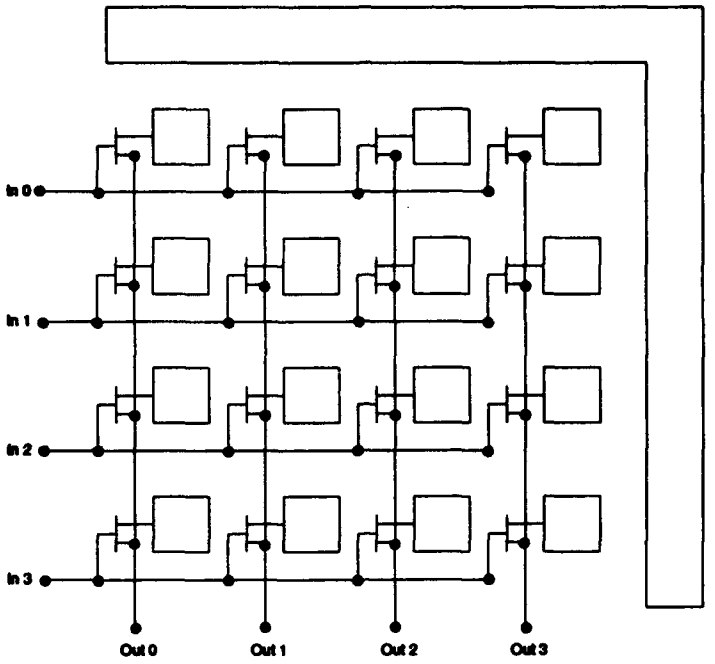


Figure 2. Schematic diagram of the Tatman/Fitzgerald array.

1.3 History of the AFIT Multielectrode array

Work on the AFIT array began with Joseph Tatman's 1979 thesis (28). For his thesis, Tatman designed a 16-electrode array using semiconductor technology. Unfortunately, Tatman was unable to successfully fabricate a working device. However, the next year, Gary Fitzgerald redesigned the array and successfully fabricated several devices using the new design (8). The devices Fitzgerald fabricated consisted of a 4 × 4 array of electrodes. A simple multiplexing scheme was used allowing the sixteen electrode device to be connected with external electronics using only nine I/O connections; four inputs, four outputs, and a reference. A schematic diagram of the Tatman/Fitzgerald array is shown in Figure 2. The electrodes are multiplexed over time by allowing each electrode to be connected to one of the four outputs. This was done using junction field effect transistors. After fabrication, the array was tested in an open air environment and found to be functioning properly.

The brain, however, rests in a fluid, the cerebral spinal fluid. This fluid is similar to a 0.9% saline solution. In order to test the chip in this environment, a simulated brain was constructed, consisting of paper towels resting in a saline solution. Testing the array with the simulated brain caused failure within a few seconds. Fitzgerald determined that a method for passivating the device from the salt water was needed. Of course, this is not required of standard electronics passivation techniques.

George German in his 1981 thesis explored methods for protecting semiconductor devices (9). His thesis, suggests two possible materials that could be used to passivate the device: polyimide, and phosphorus glass. Passivating one of the Fitzgerald arrays with polyimide, Russell Hensley and David Denton were able to successfully implant an array in a laboratory beagle (13). The implanted device survived for 17 days before it was removed from the subject. The subject, "Ricky," survived the operation and is still alive today at the age of 19.

Denton and Hensley's work validated the concept of the multiplexing techniques used in the array, showing that meaningful data could be acquired using a semiconductor array designed to study the cortical columns. However, several improvements were needed for future work. First, the array needed more electrodes. Second, array pads needed to be decreased in size to better match the size of the cortical columns. Third, better methods were needed for fabricating the arrays to improve the array's electrical characteristics. And fourth, the surgical procedure and implantation procedure needed to be improved to decrease their effect on the subject. The array developed in this and previous thesis efforts solves all of the problems above.

Following on the work of Denton and Hensley, Robert Ballantine redesigned the array in his 1983 thesis (3). The new design was a 16×16 array of electrodes to be fabricated using n-channel metal oxide semiconductor (NMOS) technology. Ballantine's design also included multiplexing circuitry similar to the design by Fitzgerald.

Further, Ballantine's design could be fabricated by MOSIS, a government service for manufacturing semiconductor devices. Following on this effort, Ricardo Turner designed a new method for implantation of the device (30), addressing the major concerns of Denton and Hensley.

Unfortunately, fabrication of the array using the MOSIS service created a new problem. MOSIS fabricated the arrays with aluminum electrodes. Aluminum corrodes when exposed to saline environments such as the cerebral spinal fluid. Therefore, a method to protect the electrodes with a chemically inert coating was needed. This coating was also required to be highly conductive to allow contact with the cerebral spinal fluid. Turner studied this problem by attempting to coat the device with several metals. He successfully coated the electrode using silver. Later thesis efforts attempted to use other metals such as platinum, and were unable to reproduce Turner's success. Turner was unable to reach implantation due to difficulties in connecting the array to the implantation package. Bonding wires continued to lose contact while a protective layer of polyimide was being added. In order to address this, the implantable package was redesigned in this thesis.

A second problem, caused by NMOS technology, was large power consumption. Power consumption will cause the array to heat up, a highly undesirable property for an implantable array. Also, MOSIS typically uses a CMOS fabrication process. Therefore, in 1989, David Szczublewski redesigned the array using complementary transistor metal oxide semiconductor (CMOS) technology (26). Unfortunately, this chip did not fully function. Pierre LeFevre then redesigned the array in his 1990 thesis (24). This design, too, did not completely function. Also in his thesis, LeFevre further explored methods for coating the electrodes. His work moved the array closer to implantation.

However, implantation requires additional work in several areas. Therefore, in the present thesis, several items were addressed. First, the array's multiplexing

circuitry was redesigned. Secondly, a reproducible method for coating the array was developed. And third, a new implantable package was designed and constructed.

1.4 Summary of Current Knowledge

Work on a semiconductor array for studying cortical columns has been performed only at AFIT. However, several other research groups have worked on fabricating semiconductor electrodes for studying the central nervous system. The work of these groups addressed many of the challenges faced in the development of the AFIT array. In particular, much of the work has focused on protecting semiconductor arrays from cerebral spinal fluid by coating the electrodes and by encapsulating the device in a protective coating.

Work on coating the electrodes has centered around the use of iridium and iridium oxide. Scientists at the University of Michigan have shown that iridium works as a coating for electrodes (2). Iridium was successfully used in several implanted packages at both Stanford University and the University of Michigan (1, 21, 22). Further studies at the University of Michigan have shown that oxidized iridium has lower impedance, and is therefore a better electrode coating (2).

Work on protective coatings has centered around the use of silicon nitride in combination with silicon dioxide. Silicon nitride is known to provide good protection from alkali ions (27), and is therefore likely to protect against the sodium and potassium ions found in the cerebral spinal fluid. Using layers of silicon dioxide and silicon nitride, successful devices have been fabricated and implanted (1, 21, 22). However, none of the devices implanted contained active transistors.

1.5 Scope

It has been over a decade since the successful implantation of the AFIT array into a subject. Therefore, the goal of this thesis was to bring the array to the point of a second implantation, and if time permitted to perform the implantation. With

the conclusion of this effort, the array is now ready for a second implantation. Time unfortunately prevents the implantation occurring as a part of this thesis.

Due to the goal of developing an implantable package, the first goal of this effort was to correct design flaws in the previous array design (24). No design changes were made other than those necessary to get the device functioning. Further, a full simulation of the array is now possible due to improved computing facilities.

The second major effort was to develop a method for passivating the arrays. This consisted of applying a metal coating to the electrodes and developing a reliable method for applying coatings of polyimide. Time did not permit experimentation with silicon nitride.

Third, this effort focused on developing and constructing an implantable package. Design of the package was based on the work of Ricardo Turner (30).

And finally, the array was tested in a simulated neural environment. Testing was done with the goal of ensuring the passivation was sufficient, measuring the expected endurance of the chip, and measuring the impedance of the circuit between the electrode and the multiplexed output.

1.6 Approach

The first phase of this thesis effort was the redesign of the array and the development of an implantation package. This consisted primarily of the addition of a new counter. Several minor wiring errors on the chip were also corrected. Finally, a thorough simulation of the chip was performed to ensure that fabrication would be successful. The array was then fabricated through MOSIS. The returned array was thoroughly tested to determine its characteristics.

The implantation package was redesigned while the chips were being fabricated. The basic design is based on the Turner's implantation package (30:2.5-2.12). The

modifications focused on the interface from the array to external driver electronics. Construction of the implantation package was done by the AFIT model shop.

Following the first phase, work was done on coating the chip using polyimide. The polyimide coating process is based on the process developed by German (9) and later improved by Turner (30). Methods for using the polyimide were first developed on silicon wafers and then performed on the actual chips.

Methods for metalizing the electrodes were also developed using standard silicon wafers. It was first necessary to determine deposition rates for both titanium and iridium. After these were determined, a lift-off technique was used to pattern the metal. Using these techniques, several of the arrays were metalized with a titanium and iridium coating.

Several chips were mounted on the implantation packages. Wire bond connections were made from the chips to the packages. Testing was then performed on a simulated brain resting in a salt water solution.

1.7 Order of Presentation

This thesis is ordered according to the steps necessary to produce an implantable package beginning from ground zero. Therefore, chapter 2 provides a review of the efforts being done at other universities. Chapter 3 discusses the design and validation of the AFIT array. Chapter 4 discusses testing the fabricated array. Chapter 5 provides the methods necessary for encapsulating the array with polyimide, and coating the array with iridium. Chapter 6 discusses the interface between the AFIT array and external electronics, including the design of the implantable package. Chapter 7 discusses testing the array in a simulated neural environment. And Chapter 8 provides conclusion with suggestions as to further work.

II. Literature Review

2.1 Introduction

As mentioned in Chapter 1, there are currently no methods for studying the cortex at the level of the cortical column. One notable effort was made by DeMott in 1966 (6). DeMott bundled together 400 thin wires. The bundle was nearly square, with wires spaced approximately $250\mu m$ from center to center. In his work, DeMott recorded EEG signals using the array. However, little other work has been done on developing devices to study the brain at the level of the cortical column. Using semiconductor technology, the AFIT multielectrode array will be able to study the brain at the cortical column level.

Unfortunately, semiconductor devices do not function well when exposed to the environment of the central nervous system. This is because the central nervous system rests in a fluid, the cerebral spinal fluid (CSF). The CSF is necessary for the neurons to communicate and live. Neurons use ions in the CSF for communications (5). These ions consist primarily of sodium, Na^+, and potassium, K^+. For semiconductor devices, this environment is very detrimental and can cause failure of any inadequately protected device within a matter of seconds, as indeed occurred with the Tatman/Fitzgerald array in its tests with the simulated brain (8:73-86).

Several other researchers are working on developing neural arrays using semiconductor technology (1, 2, 11, 14, 21, 22, 31, 32). While their devices are not aimed at studying signals from cortical columns, their work faces the same difficulties that must be dealt with in developing the AFIT array. The problem of protecting semiconductor devices from the CSF consists of two problems. First, electrodes must not corrode in the CSF. Second, the device must be insulated from the liquid and the alkali ions. Therefore, the next two sections provide a discussion of these areas and how this relates to the AFIT array.

2.2 *Protection of the Electrodes*

The exposed electrodes must be composed of a metal that will not react with the CSF. Further, in the case of stimulating electrodes, high current densities are required of the electrode metal. Several metals have been used in the past that provide this capability, including gold, platinum, silver, and iridium.

The original AFIT array was fabricated using gold electrodes. However, Kabrisky reports that anomalous spikes were recorded that were most likely caused by the junction between the gold and the CSF (18). More recently, gold has been used by Boppart *et al.* in their fabrication of flexible electrode arrays (4). Their arrays were designed for use with slices of cortical tissue. The arrays were successfully tested on slices from the hippocampus of several rats. This suggests that gold can be successfully used for recording neural signals. However, the tests were conducted on tissue slices and not on living animals.

Gold, as well as platinum and silver, require that large electrodes be used in order to support the current necessary for stimulation (32:125). However, it is not always possible to have large electrodes. Further, current flow over a planar surface is not uniform (32:125). This can cause damage to the electrodes in areas where the current density is high. Therefore, for small stimulating electrodes, gold is not an ideal metal.

Most other researchers have chosen to use iridium or iridium oxide (1, 2, 11, 14, 21, 22, 31, 32). Iridium is a noble metal and is therefore very inert. Further, iridium is capable of carrying high current densities. Iridium can be used directly or can be activated by oxidation.

Anderson et al., at the University of Michigan, tested both oxidized, or activated, and non-oxidized iridium (2). Oxidation of the iridium is performed by cycling a triangle wave voltage potential between the electrode and a reference electrode, while both electrodes are immersed in a sulfuric acid solution. This process

forms a uniform layer of iridium oxide on the electrode. Anderson's test have shown that iridium oxide is capable of carrying higher current densities, and is therefore preferable for stimulating electrodes. In their tests, up to 8 million pulses were ran through both activated and non-activated electrodes. The electrodes impedance remained constant throughout the test. Further, the electrode showed no signs of delamination from the underlying layers of polysilicon (2:698).

Ziaie, *et al.*, have developed a neuromuscular stimulator (32). This device contains several large electrodes for stimulation of neuromuscular tissue. Their electrodes were created using activated iridium electrodes. For their stimulators, Ziaie *et al.* required larger currents than used in other work. Therefore, it was necessary for them to increase the size of their electrodes. However, they noted that charge densities are not uniform across planer arrays (32:125). Therefore, it was necessary for them to create an array of 20 μm by 20 μm electrodes that were electrically connected to an underlying pad of polysilicon. This causes the current densities to be uniform over the smaller exposed areas while multiple exposed sites connected to the same electrode allowed the larger currents required.

Also at the University of Michigan work has been done with regeneration arrays (1). This work is currently using activated iridium oxide due to the decreased impedance of the activated iridium and the high charge current density that can be passed through the iridium sites (1).

At Stanford, regeneration arrays using iridium electrodes have been tested *in vivo* (21, 22). An 8×8 array of electrodes has been created. Each electrode is next to a thru hole that passes through the device as seen in Figure 3. This work did not activate the iridium electrodes. However, successful recording and stimulation was performed.

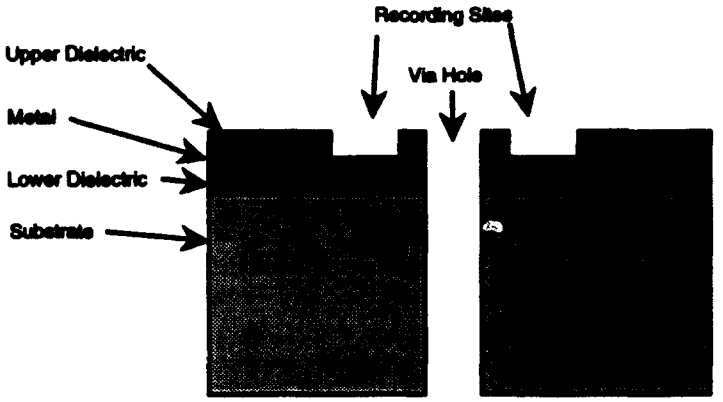


Figure 3. Electrode site of a regeneration array (22).

2.3 Passivation of the Device

Several researchers have reported success at fabricating passive neural electrodes using semiconductor devices (1, 2, 21, 22). However, very little success has been recorded with active devices. This is caused by the difficulty in protecting active circuitry from the alkali ions in the CSF. In his thesis, George German suggested several potential methods for protecting semiconductor devices. Most notable of these choices were polyimide and silicon nitride (9). Silicon nitride has been used by several researchers in their efforts to fabricate neural electrodes (14, 21). Polyimide has been used here at AFIT, as well as by several researchers at other universities (4, 13).

2.3.1 Silicon Nitride Passivation. George German reported that silicon nitride showed promise in protecting semiconductor devices (9). It is known that silicon nitride will protect devices from the alkali ions present in the CSF (27). However, German was unable to sputter silicon nitride layers free from pinhole defects (9). These pinhole defects were caused by the method used to deposit the silicon nitride on the chips. Recently, several works have discussed success using silicon nitride passivation layers (1, 2, 14, 21, 22, 31). In general, a modified form of chemical vapor deposition, such as plasma enhanced chemical vapor deposition, is used to

deposit a uniform layer of silicon nitride. Of particular interest is the work that has been done at the University of Michigan and a separate work done at Stanford University (1, 14, 21, 22).

At the University of Michigan, researchers have generated micro-probe electrodes, and regeneration electrode arrays. Their coating system consists of three layers: an outer, or upper dielectric; a metal layer; and an inner, or lower, dielectric. The upper and lower dielectric layers provide the insulation to prevent shorts and protect from the alkali ions. These layers are composed of silicon nitride sandwiched in between two layers of silicon dioxide (1, 2). In the regeneration array, both dielectric layers consist of 3000 Å of silicon dioxide, followed by 1500 Å of silicon nitride, followed by 3000 Å of silicon dioxide. For the micro-probe electrodes, the lower layer of silicon dioxide is 100 Å thick, followed by 2000 Å of silicon nitride, followed by 8000 Å of silicon dioxide. The upper and lower dielectric layers are again similar. Anderson *et al.* notes that the relative sizes of the layers are important to prevent warping of the micro-probe array (2).

Researchers at Stanford have chosen a different method (21, 22). They also use upper and lower dielectric layers to protect a metal layer. However, their lower dielectric consists of 5000 Å of silicon dioxide, and the upper dielectric consists of a 1μm layer of silicon nitride. The silicon nitride should prevent the permeation of alkali ions, while the silicon dioxide layer will isolate the metal layer from the silicon substrate and any active circuitry.

Both groups have been able to successfully fabricate passive electrode arrays, and test the arrays in living subjects. However, neither group has reported success with active arrays. Work is proceeding in this area, however.

2.3.2 Polyimide Passivation. In his thesis, German reported that polyimide also had the properties required for protecting active devices (9). Polyimide, however, is easier to apply than silicon nitride. Therefore, Denton and Hensley used

polyimide for coating the array that was implanted (13). Other researchers have also used polyimide (4).

Boppart *et al.* have designed and fabricated a flexible array using polyimide layers to protect an internal metal layer (4). The array is fabricated by laying down a thick (10 μm) layer of polyimide first. On top of this layer, a thin layer of titanium (30 Å) followed by 750 Å of gold. Finally, a top layer of polyimide is deposited (2 μm). The lower layer of polyimide is DuPont Pyralin 2525, and the top layer is DuPont Pyralin PI-2555. Several holes are etched through the array to allow fluids to pass through the array. As mentioned in the previous section, these arrays have been used for recording from neural slices with good results (4).

This method creates a flexible electrode array for recording from neural slices. However, the method does not permit the incorporation of active transistors on the device. Boppart *et al.* note that polyimide is a good, but not perfect, coating for electrode arrays. Polyimide has been shown to gradually deteriorate over several months. This is most likely attributed to a slow absorption of water by the polyimide. This will eventually cause failure of the electrode array. However, polyimide is easier to work with than silicon nitride.

2.4 Conclusion

Most of the recent work being done on neural semiconductor electrodes has focused become focused around the use of iridium electrodes and silicon nitride passivation (1, 2, 11, 14, 21, 22, 31, 32). Polyimide has been used in some research (4, 13). However, it is known that the polyimide will absorb water slowly, eventually causing failure of any active circuitry.

Iridium has been found to be an ideal metal for stimulating electrodes (32). Therefore, it has been decided to use iridium for the AFIT multielectrode array.

Unfortunately, the resources required for applying silicon nitride to the AFIT array are not currently available. Facilities for applying coatings of polyimide are

available at the Cooperative Electronics, Materials, and Processes Laboratory at AFIT. Therefore, while polyimide is not the ideal passivation material, it will be used for passivating the AFIT array. Note that polyimide should be adequate for extended periods of over 1 month.

The design of the AFIT array is unique. No other researchers have reported working on multiplexed 2-dimensional surface arrays for studying the cortex at the level of the cortical column.

III. Design of the Multiplexed Electrode Array

3.1 Design Considerations

The AFIT multielectrode array, or the 'brain chip', is intended to study the brain at the level of the cortical column. The goal of the research is to implant two devices in different areas of the visual cortex (V1 and V2). By then providing stimulus into V1 and recording the data in V2, it may be possible to determine some characteristics of the interconnection matrix between the two areas. This information would make it possible to determine the nature of the data transformation that occurs from V1 to V2 (20).

In order to allow stimulation and recording from a large number of individual cortical columns, the brain chip must meet the criteria listed in Table 1.

As was discussed in the introduction, an array was designed using semiconductor technology to meet the above goals (3, 9, 13, 24, 26, 28, 30). The latest design of the array, was done using a computer aided design package called MAGIC. In MAGIC, a designer lays out the design of an integrated circuit. MAGIC is then used to output the information about the circuit necessary for fabrication. This information is sent electronically to a MOSIS for commercial fabrication. Commercial companies are better able to control the fabrication process. Thus they can fabricate devices with smaller feature sizes, more uniform device characteristics across an entire chip, and achieve high yields. Commercial fabrication was first suggested by Denton and Hensley due to the fact that the Fitzgerald arrays had differing characteristics for each individual transistor (13). Robert Ballantine first used commercial fabrication for his 16 × 16 array with NMOS circuitry (3).

Shown in Figure 4, the AFIT array design consists of 256 electrodes laid out in a square 16 × 16 array. Each electrode has circuitry allowing it to be enabled or disabled. The array also contains circuitry to cycle through the array enabling each

Table 1. Requirements for the AFIT multielectrode array

Requirement	*Reason*
Small size	Approximately match the size of individual cortical column
Bidirectional Current Flow	Allow both stimulation and recording of the cortex
Small number of I/O connections	Difficulty in making connections from inside the cranium to external circuitry
Number of I/O connections not dependent on the number of electrodes	Allows the number of electrodes to be increased without increasing the number of connections
Capability to individually address the electrodes	Allows stimulation and recording to individual locations of the cortex

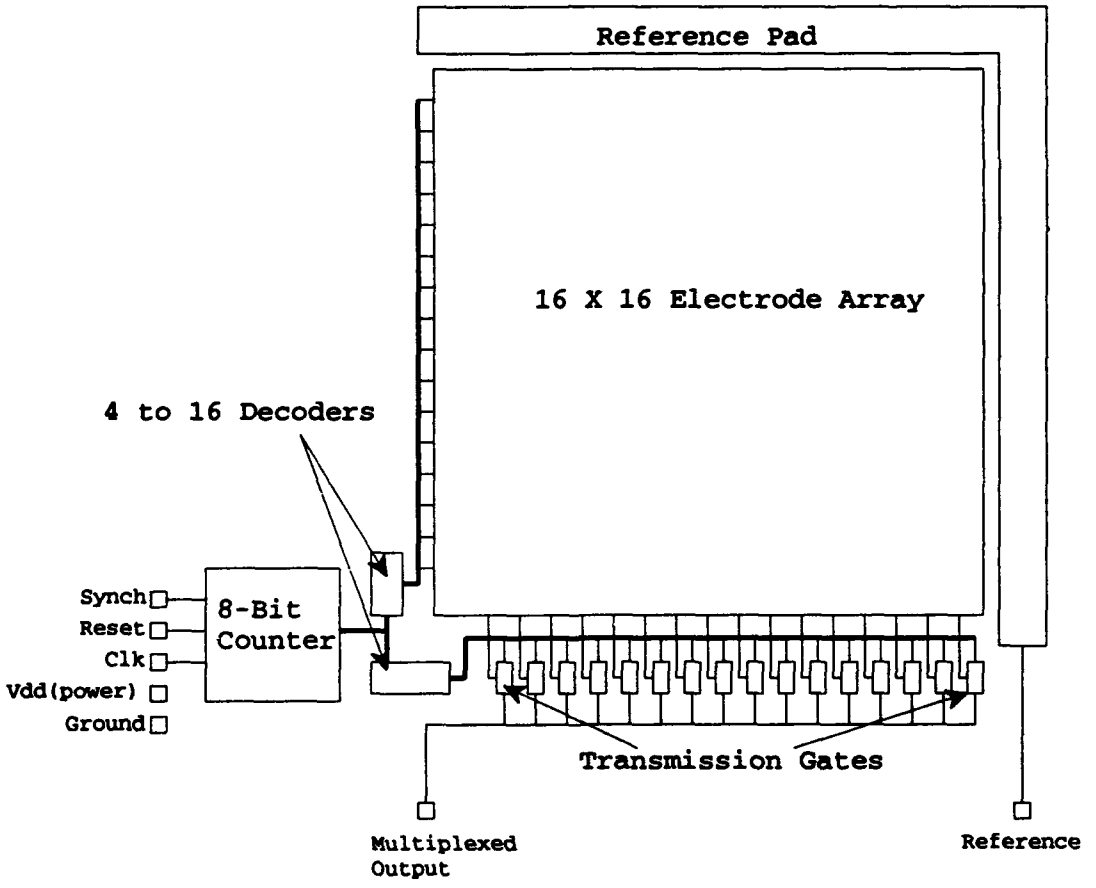


Figure 4. Stylized version of the AFIT Multielectrode array

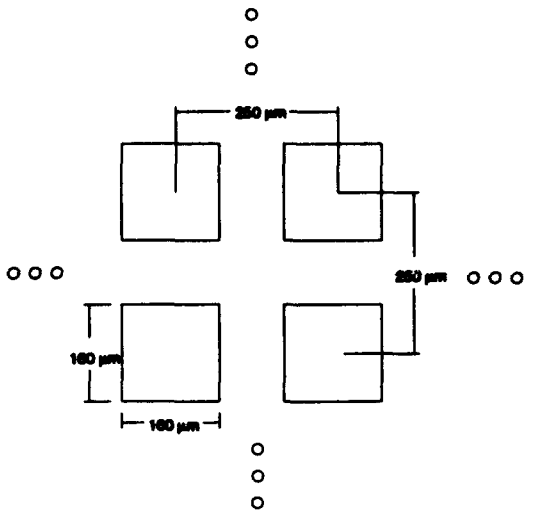


Figure 5. Electrode spacing

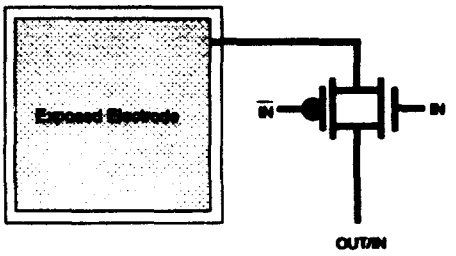
electrode of the array individually. The following sections provide more information on the design of the electrodes and the controlling circuitry.

3.2 Electrode Array

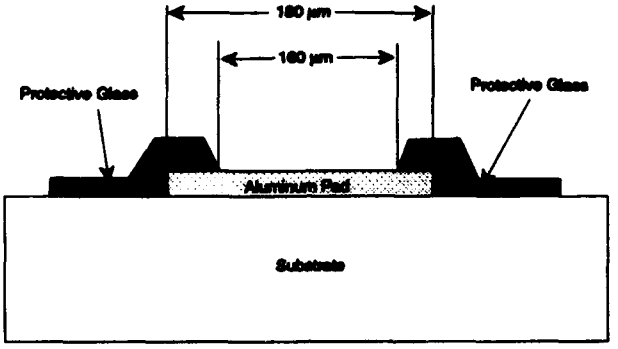
The electrodes are equally spaced to form a square 16 × 16 array of electrodes. The electrodes are spaced as shown in Figure 5 with each electrode having an exposed area of 160 μm square and a center to center spacing of electrodes of 250 μm. In Figure 6, the layout of each individual electrode and the associated circuitry can be seen.

The actual electrode has several layers. First, is a $180\mu m \times 180\mu m$ aluminum pad. Above the pad, is a layer of glass for passivating the device. This layer is necessary to protect the device from an open air environment. However, the protective glass would prevent the aluminum electrode from making contact with the cerebral spinal fluid. Therefore, a $160\mu m$ square hole has been cut through the protective glass layer to expose the underlying aluminum pad.

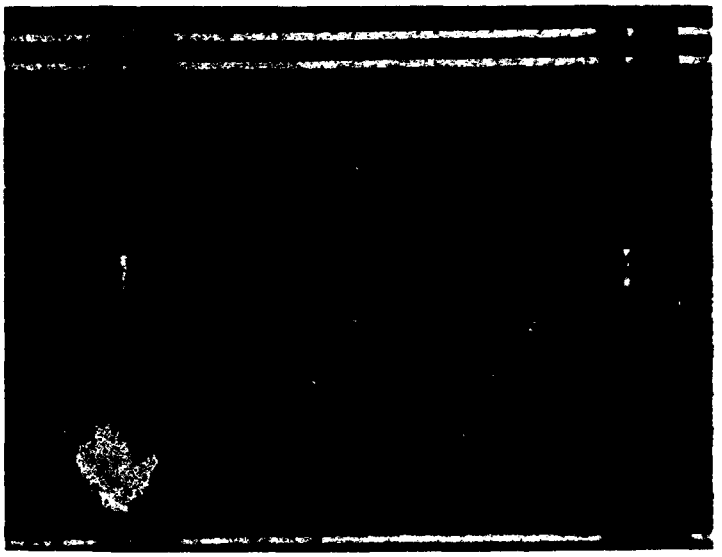
The aluminum pad is directly connected to the driver circuitry. This circuitry consists of a pair of MOS transistors. One of the transistors, is an *n*-channel tran-



(a)



(b)



(c)

Figure 6. (a) Schematic of an electrode site. (b) Side view of the electrode. (c) Picture of a fabricated electrode.

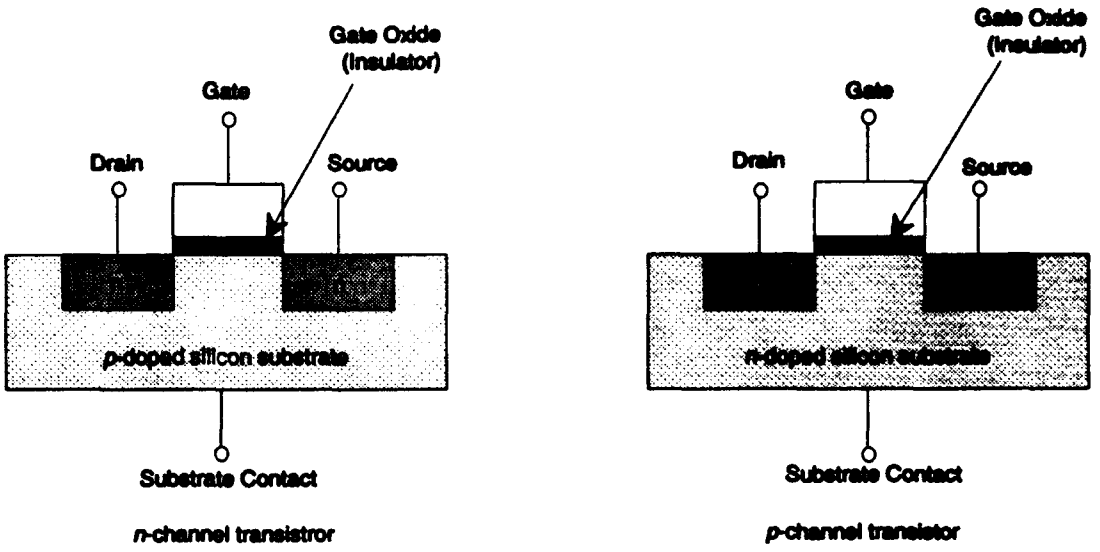


Figure 7. Diagram of fabricated n- and p-channel MOS transistors.

sistor, and the other is a p-channel transistor. Figure 7 shows a diagram of what n-type and p-type transistors look like after fabrication. With a metal oxide semiconductor structure, the voltage between the gate and the substrate creates a channel between the source and the drain of the transistor. For an n-channel transistor, the p-doped substrate is grounded. Applying a logical high voltage (V_{DD}) to the gate will then generate an electric field between the gate and the substrate contact. This field causes an inversion layer to form in the p-type substrate. The n-type inversion layer will connect the source to the drain allowing current to flow. For a p-channel transistor, this is exactly opposite with the substrate connected to a high voltage, and thus grounding the gate will generate a p-type channel from the source to the drain. In effect then, the MOS transistor can be seen as a switch. When the appropriate voltage is applied to the gate, a channel is created between the source and the drain, and current can flow. When the voltage of the gate is similar to the voltage of the substrate no channel exists and the switch is closed. Using the transistors as a switch, it is possible to enable or disable each individual electrode. This is done by connecting together a n-type and a p-type transistor, such that sources and drains

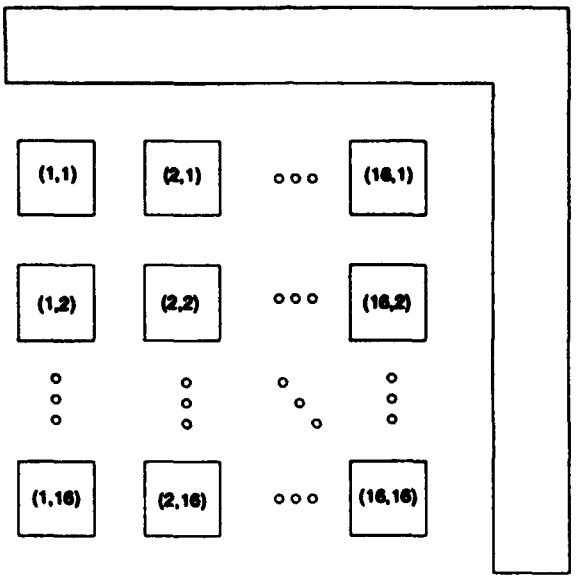


Figure 8. Electrode numbering scheme.

of the two transistors are connected together. The electrode is then connected to the source of the two transistors. The drain provides an output that is connected to the electrode when the transistors are properly enabled, but is disconnected from the electrode when the transistors are not enabled. To enable the electrode, a high voltage (V_{DD}) is applied to the gate of the *n*-channel transistor, and a low voltage (ground) is applied to the gate of the *p*-channel transistor.

With this design, each individual electrode is capable of being switched on or off. It is therefore possible to connect the outputs of several of the electrodes together onto a single bus, and then by enabling only one of the electrodes on the bus at a time, several electrodes can share a single I/O connection. Further, because of the nature of the transistors, it is possible for current to flow either into or out of the electrode. Therefore, the activated electrode is capable of both recording and stimulation.

As mentioned, it is now possible to multiplex the output of several electrodes onto a single I/O channel. Considering the electrode array to be numbered as shown in Figure 8. The outputs from electrodes (x,1) through (x,16) are connected together,

to generate 16 I/O lines for all 256 electrodes. Thus there is one output for each column of the array. Further, connecting the inputs from electrodes (1,x) through (16,x) generates 32 input lines, or 2 inputs for each row of electrodes. However, the input to the *p*-channel transistors is the inverse of the input to the *n*-channel transistors. Therefore, one input for the *n*-channel transistors is needed. This input is inverted and sent to the *p*-channel transistors. This reduces the number of inputs to 16.

Therefore, the array currently has 16 inputs, and 16 I/O connections for 256 electrodes. Enabling one of the 16 inputs, by setting the input voltage to a logical high value (V_{DD}) connects one electrode to each of the 16 I/O lines.

3.3 Reference Pad

Voltage potentials must be measured as the change in potential from one point in reference to a second potential. With the brain chip, potentials will be measured with reference to a local average potential. Therefore, it is necessary to provide a reference electrode. The reference electrode is the large L-shaped pad shown in Figure 4.

The reference pad is similar in construction to the aluminum electrode pads. It consists of a large aluminum pad, 180 μm wide, that runs for 4308 μm across the top of the array and another 4060 μm down the side of the array. A cut is made in the chips protective coating to expose the aluminum pad. As with the electrodes, this cut is 160 μm wide.

Since the reference electrode will be used in measuring all of the potentials from the individual electrodes, a direct connection from the reference electrode to the outside of the chip is provided. Therefore, with the 32 connections currently necessary for the electrodes, plus a power line, a ground line, and the reference connection it is necessary for 35 I/O connections from the chip.

3.4 Multiplexing Circuitry Design

As described in the previous section, the electrode array requires 35 connections. While this is significantly less than the 256 electrodes, it is still a large number of wires to bring out of the subject's cranial cavity. Further, it is still necessary to have $2n$ I/O connections for n^2 electrodes. While this is a significant improvement, it still limits the number of electrodes that can be added to the array. Therefore additional multiplexing circuitry is designed to multiplex the 16 outputs into a single output line, and to provide signals to drive the 16 input lines of the electrode array.

3.4.1 Multiplexing the output lines. Utilizing the same type of circuitry as was used with the electrodes, the individual column outputs are connected to a single I/O connection. A pair of transistors one p-type and one n-type are connected together to form a transmission gate. An inverter is also added to allow a single input to enable or disable the gate.

The design now has a single I/O connection. However, there are two 16 channel inputs. It is important to note that only one row input and one of the pass gates can be enabled at any given time, and that by choosing which of these lines is enabled, any of the 256 electrodes is connected to a single I/O connection.

3.4.2 Driver circuitry. On chip circuitry is provided to control the 32 input lines. First, two 4 to 16 bit decoders were used. A decoder simply takes a n-bit binary number and enables one of 2^n output lines. Note that this will not only drive 16 input lines with a 4 bit input, but it will ensure that one and only one of the lines is enabled at any time. Therefore, by using two decoders a single 8-bit input can drive all 32 of the electrode array input lines. A picture of the fabricated decoder is provided in Figure 9.

It is now possible to drive the two decoders using an 8-bit counter. Previous thesis efforts have had difficulties developing successful counter circuitry. Therefore,

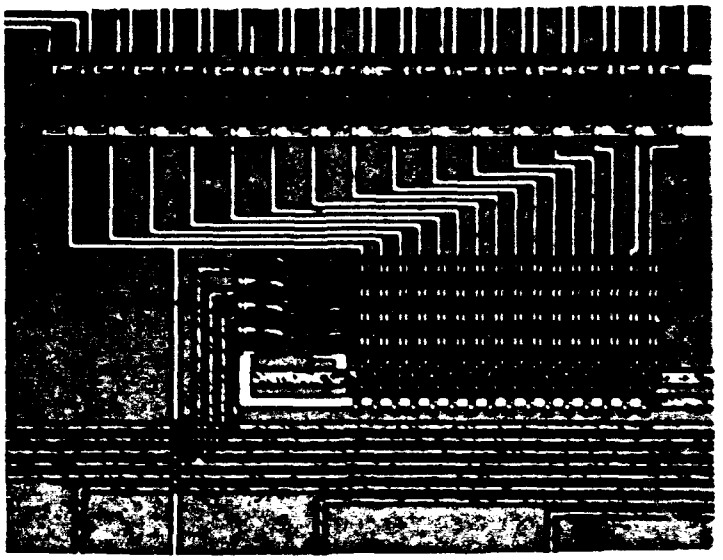


Figure 9. Fabricated 4 to 16 decoder

with the help of a VLSI student at AFIT, Bill O'Connor, a resetable 8-bit counter was designed using standard cell technology. Standard cell technology takes a simple logic design input and generates a VLSI circuit that meets the logical specification of the design. To generate the MAGIC layout, standard cell technology relies on 'cells' that have been previously tested and fabricated. Therefore, standard cell designs are highly reliable. Further, standard cell technology can be implemented quickly. This allowed a fabrication of the brain chip early in the thesis cycle. Figure 10 shows a picture of the fabricated counter.

With the addition of the counter and the decoders, all 32 of the electrode array inputs can be driven with only a power, ground, and clock inputs for the counter. A synch output was also added to the system. This connection provides a low output whenever the counter has an output value of zero. This output can be used to aid in de-multiplexing the signal.

3.5.1 Well Checking. As shown in Figure 7, a MOS transistor has four connections; drain, gate, source, and substrate. The substrate connection is very important for the proper operation of the transistor. In VLSI circuits, substrate contacts are made by means of a well contact.

MAGIC provides a means to check to ensure that there is a well contact located close enough to each transistor. Running this check on the brain chip generated several errors. The majority of the errors were corrected. However, the 4 to 16 bit decoders currently do not have well contacts close enough to the center of the circuit. Fortunately, the MAGIC well checking system follows a simple rule of thumb in determining errors. It was determined at this point, that the decoder would function properly despite the location of the well contacts.

3.5.2 ESIM. In order to perform a logical analysis of the design, the program ESIM was used to simulate the entire brain chip. ESIM simply assumes that all transistors are either on or off, and therefore simulation with ESIM ensures that the design is logically correct, and all the transistors are correctly wired together. However, ESIM will not simulate any of the circuit characteristics, and therefore a design that functions correctly in ESIM is not guaranteed to function correctly after fabrication.

In order to perform an ESIM simulation, it is first necessary to generate a **.sim* circuit specification file. To create the specification file, a **.ext* file is created using the MAGIC command 'ext'. Running *ext2sim* on a **.ext* file generates a **.sim* specification file. This file provides the circuit design information needed by ESIM.

After creating the **.sim* file, it is necessary to create a simulation file. This file contains the information telling ESIM what the simulation will do. This includes telling ESIM which outputs to watch, and how to set the inputs. ESIM will allow the user to set or watch any value in the circuit that has been properly labeled.

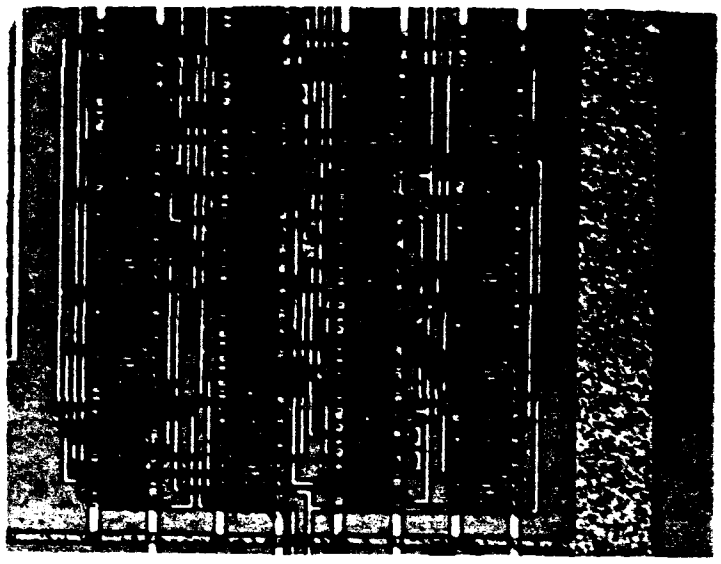


Figure 10. Fabricated 8-bit counter

Table 2. Connections for testing the AFIT array

Number	*Connections*
8	8-bit counter outputs
16	Individual Column Outputs
1	Output from one of the 4 to 16 bit decoders

3.4.3 Additional Interface Connections. In order to aid testing of the brain chip after fabrication, the 25 connections listed in Table 2 were also provided.

3.5 Validation of the design

Validation of a VLSI design requires analysis of several aspects of the circuit. First, it is necessary to ensure that well contacts have been placed close enough to all of the transistors in the design. Second, a logic analysis should be performed. And finally, SPICE circuit analysis should be performed.

ESIM was used to verify the proper function of the brain chip design. In particular, it was used to verify that the counter was properly connected, and that signals placed on the electrodes would properly pass to the multiplexed output. It was possible to meet these goals with a single simulation. This simulation provided a power, a ground, a clock, and a reset to the chip. Inputs are also placed on several of the electrodes. The simulated outputs of the counter, as well as the multiplexed output were then evaluated. However, as mentioned earlier, this simulation only verifies that the chip is properly wired, and that the logical design is correct. The output from the ESIM simulation is not provided here since the information obtained can also be found in the SPICE simulation output. It is important to note here that ESIM is used first because it takes very little time to run. SPICE simulations require significant computational time, and therefore are only performed after ESIM has verified the design and connectivity of the circuit.

3.5.3 SPICE. Unlike ESIM, SPICE is a circuit level simulator. SPICE actually models the individual components of a circuit, and solves the circuit equations to determine the state of the circuit. To further ensure that its results are accurate, SPICE uses model parameters based on previous fabrication runs. However, simulation with SPICE is very computationally intensive. Fortunately, computers are have become fast enough to allow the simulation of fairly large circuits such as the brain chip.

AFIT uses a commercial version of the SPICE program called HSPICE. Running the program *ext2hsp* on the **.ext* file generates a **.sp*. This file contains the circuit specification of design in a SPICE input format.

HSPICE simulation was used to show low voltage signals propagating from the electrodes to the output. This simulation provided some estimate as to the expected performance of the brain chip. However, the SPICE model used is accurate for transistor transitions from 0 volts to 5 volts. Since the simulations were based

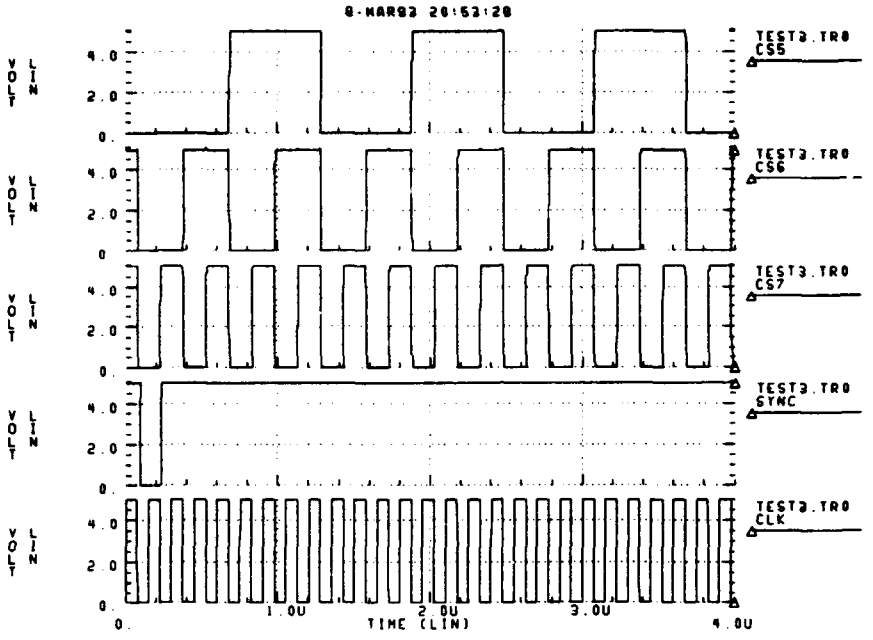


Figure 11. SPICE output showing several of the clock signal outputs, and the output of the synch. Note that all clock lines transition at the same time.

on millivolt inputs, the actual performance of the circuit will vary from the simulation results. Note that due to the computationally intensive nature of HSPICE, all simulations were fairly short. However, the simulations do fully verify the brain chips design. Figure 11 shows an HSPICE plot of several of the counter outputs and the synch output. Figure 12 shows HSPICE simulation results for a signal that is propagating through the array from the (1,1) electrode to the multiplexed output. For this simulation, the reset line of the chip is set to V_{DD} so the (1,1) electrode is continually selected.

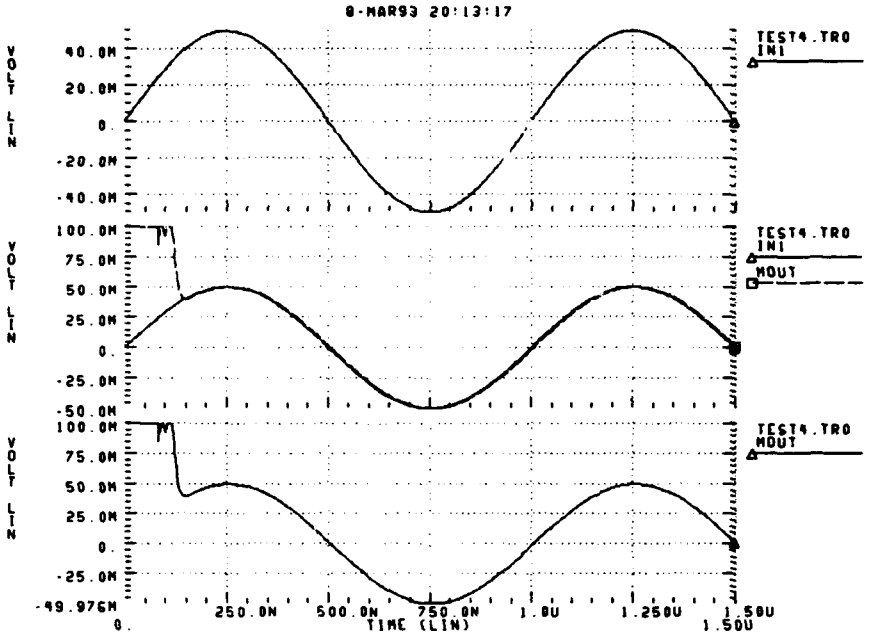


Figure 12. SPICE simulation output showing a signal propagating from a selected electrode to the multiplexed output.

3.6 Conclusions

The design discussed in this chapter has evolved throughout the history of the AFIT array. Most of the design was done in previous thesis efforts, as described in the introduction. However, in this thesis, a counter has been successfully added to the chip and minor bugs in the design have been fixed.

This design meets all of the specified goals for the chip. The brain chip is capable of individually recording from, and stimulating 256 electrodes. Further, the number of I/O connections, is no longer dependent on the number of electrodes. Therefore, it is possible to build an even larger array without increasing the number of I/O connections that are necessary.

Finally, the brain chip has been thoroughly simulated. This simulation ensures that there are currently no design flaws in the system. This simulation provides reasonable certainty that any fabricated device will properly function. However, as mentioned, simulation is not perfect, and testing the returned chips is necessary.

IV. Testing the AFIT Multielectrode Array

Before proceeding with developing encapsulation methods for the brain chip, it was first necessary to determine if the device was functioning properly, and to determine the electrical characteristics of the individual electrode sites. To aid in the testing of the AFIT array, two of the fabricated chips were packaged in a 64-connection (PGA) pin grid array package. The packaged chips are seen in Figure 13. The bonding diagram for the packaged chips is provided in Appendix A.

4.1 Testing the Functionality of the AFIT array

Determining the functionality of the brain chip required showing that the counter was functioning, finding the minimum operating voltage of the counter, and finding the maximum operating frequency of the counter. Further, it was necessary to show that a signal on the input of a selected electrode would propagate to the output electrode, and that all row and column circuitry was properly functioning.

4.1.1 Verification and analysis of the counter performance. Analysis was done by using a pulse generator to provide an input clock to the brain chip and then examining the 8 counter outputs. For all tests, the pulse generator provided a 50% duty cycle square wave. Tests were run initially with a clock having a peak-to-peak voltage of 5 volts and an input frequency of 100 kHz. V_{DD} was also initially set to 5 volts.

After examining the output of the 8 counter outputs, it was clear that the counter was functioning as expected. The output of the synch circuit was also examined and found to be properly functioning.

To determine the maximum frequency that the counter can operate at, the frequency of the input clock was increased until the output clock no longer provided a square wave. V_{DD} was set at 5V throughout this testing. The maximum frequency

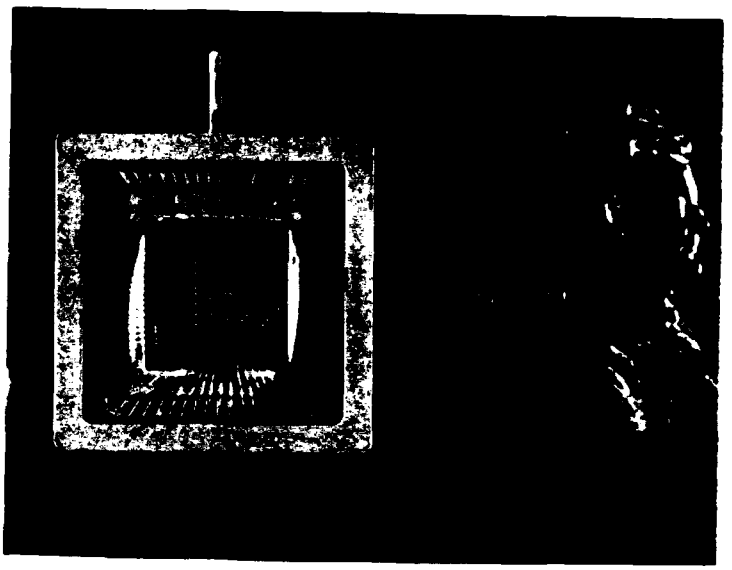


Figure 13. The brain chip packaged in a 64-pin PGA package

of the clock was determined to be:

$$f_{max} = 1.1MHz$$

However, operating at this frequency, the high frequency outputs of the counters do not form a well defined square wave, and therefore, the chip should be run at a speed well below this value.

Signals generated by the brain are typically on the order of 30 Hz. Therefore, the minimum sampling rate necessary, the Nyquist rate, is 60 samples per second. Increasing this to a comfortable 100 samples per second, the highest frequency output of the counter would be (256 electrodes) $\times$(100 samples a second per electrode), or 25.6 kHz. This is well below f_{max}.

To determine the minimum operating voltage, both V_{DD} and the peak-to-peak voltage of the input clock were decreased until the counter output was no longer providing an acceptable clock pulse. The clocks frequency was returned to 100 kHz..

Using this method, the minimum value of V_{DD} was determined to be:

$$V_{DD,min} = 1.6V$$

However, as with the frequency limit, the counter outputs are not as well defined near 1.6 volts. At voltages above 2.5 volts, the counter outputs appear normal. However, for typical operation, the brain chip will be run with an input voltage of 3.5 volts. At 3.5 volts, the counter functions cleanly, but power consumption is significantly reduced. During operation with V_{DD} set to 5 volts, the chip draws an average current of 0.049 amps. Therefore, the average power consumption is 250 milliwatts. This value decreases as V_{DD} is decreased.

4.1.2 Verification of the electrodes. Verification of the electrodes began by first providing an 50 mV peak-to-peak input signal to the (1,1) (note electrode numbering is the same as was used in Figure 8) electrode while the RESET was connected to V_{DD}. After verifying that a signal would propagate from this electrode to the multiplexed output, it was necessary to verify that each row and column were functioning properly. This was done by providing an input voltage to 16 electrodes along a diagonal. The electrodes used were (1,1),..., (x,x),...,(16,16). Examining the multiplexed output, it was clear that a signal was propagating through from the stimulated electrode to the multiplexed output for each of the 16 diagonal electrodes. Further, the output of an electrode from each row, and each column has been successfully verified. After performing these simple tests to ensure the chip was functioning, further testing was done to measure the impedance of the circuit from the electrode to the multiplexed output.

4.2 Characterization of the Electrodes

After determining that the circuit was functioning properly, more detailed information about the connection from the individual electrodes to the multiplexed

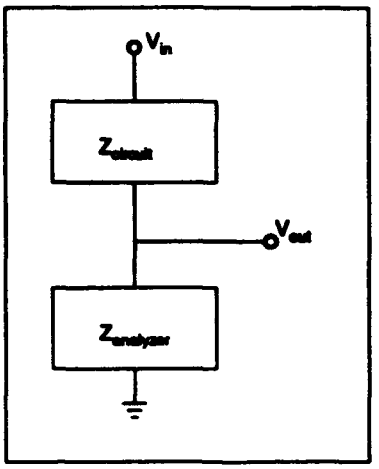


Figure 14. Impedance analyzer circuit

output was desired. In particular, the characteristic impedance of the circuit and the isolation impedance between the electrodes was desired.

4.2.1 Individual electrode impedance. The impedance of the electrodes was determined through the use of a Hewlett Packard 4192A impedance/gain phase analyzer. The impedance analyzer provides an input signal to one end of a circuit, and measures the output at the other end of the circuit. The analyzer then can measure either the impedance of a circuit, or the transfer function of the circuit. Due to the active devices in the circuit, analysis was done by measuring the transfer function through the circuit. From this information, the characteristic impedance of the circuit can be determined by considering the system to be a simple voltage divider as seen in Figure 14.

Using the equation below,

$$V_{out} = V_{in} \times \frac{Z_{analyzer}}{Z_{analyzer} + Z_{circuit}}$$

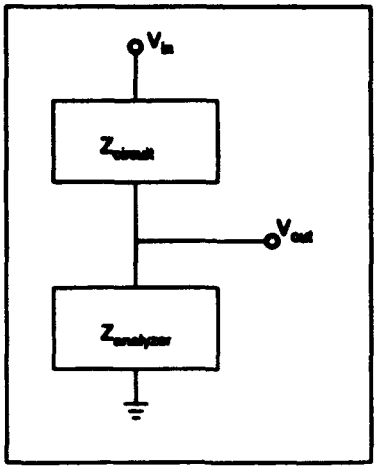


Figure 14. Impedance analyzer circuit

output was desired. In particular, the characteristic impedance of the circuit and the isolation impedance between the electrodes was desired.

4.2.1 Individual electrode impedance. The impedance of the electrodes was determined through the use of a Hewlett Packard 4192A impedance/gain phase analyzer. The impedance analyzer provides an input signal to one end of a circuit, and measures the output at the other end of the circuit. The analyzer then can measure either the impedance of a circuit, or the transfer function of the circuit. Due to the active devices in the circuit, analysis was done by measuring the transfer function through the circuit. From this information, the characteristic impedance of the circuit can be determined by considering the system to be a simple voltage divider as seen in Figure 14.

Using the equation below,

$$V_{out} = V_{in} \times \frac{Z_{analyzer}}{Z_{analyzer} + Z_{circuit}}$$

it is possible to solve for $Z_{circuit}$ as shown.

$$Z_{circuit} = \left(\frac{V_{in}}{V_{out}} - 1\right) \times Z_{analyzer}$$

Figure 15 shows the gain phase plots for for the electrode (1,1) which is selected while the RESET is held to V_{DD} keeping the electrode selected. This allows an analysis of the circuit impedance for an individual electrode, as well as the measurement of the isolation impedance of the non-selected electrodes. For all testing, V_{DD} was set to 5V and the frequency was at 100 kHz. The plots were obtained using an input impedance, $Z_{analyzer} = 50\Omega$. Using the average gain of -43 dB, $\frac{V_{out}}{V_{in}} = .0136$. Using these values to solve for the impedance of the circuit yields the value below.

$$Z_{circuit} \approx 3.6k\Omega$$

It is important to note several points here. First, the magnitude of the impedance will decrease with increasing frequency. Secondly, the circuit path passes through several active circuits. The impedance through these devices will vary with the gate to substrate voltage, and the source to drain voltage. Because of this, the value of $3.6k\Omega$ should be considered only as an approximate value, and not as the exact impedance of the circuit at any time.

4.2.2 Electrode to electrode isolation. Isolation of the non-connected electrodes was also determined using the impedance analyzer. A circuit was formed with one connection from the impedance analyzer on an electrode and the other on the multiplexed output. Tests were done on the 3 adjacent electrodes. One electrode was in the same row as the selected electrode, one was in the same column, and one was in neither the same row nor the same column. As seen in Figure 16, the isolation impedance, or the impedance between a non-selected electrode and the output, was over 100 times greater than the impedance from the selected electrode. It is also

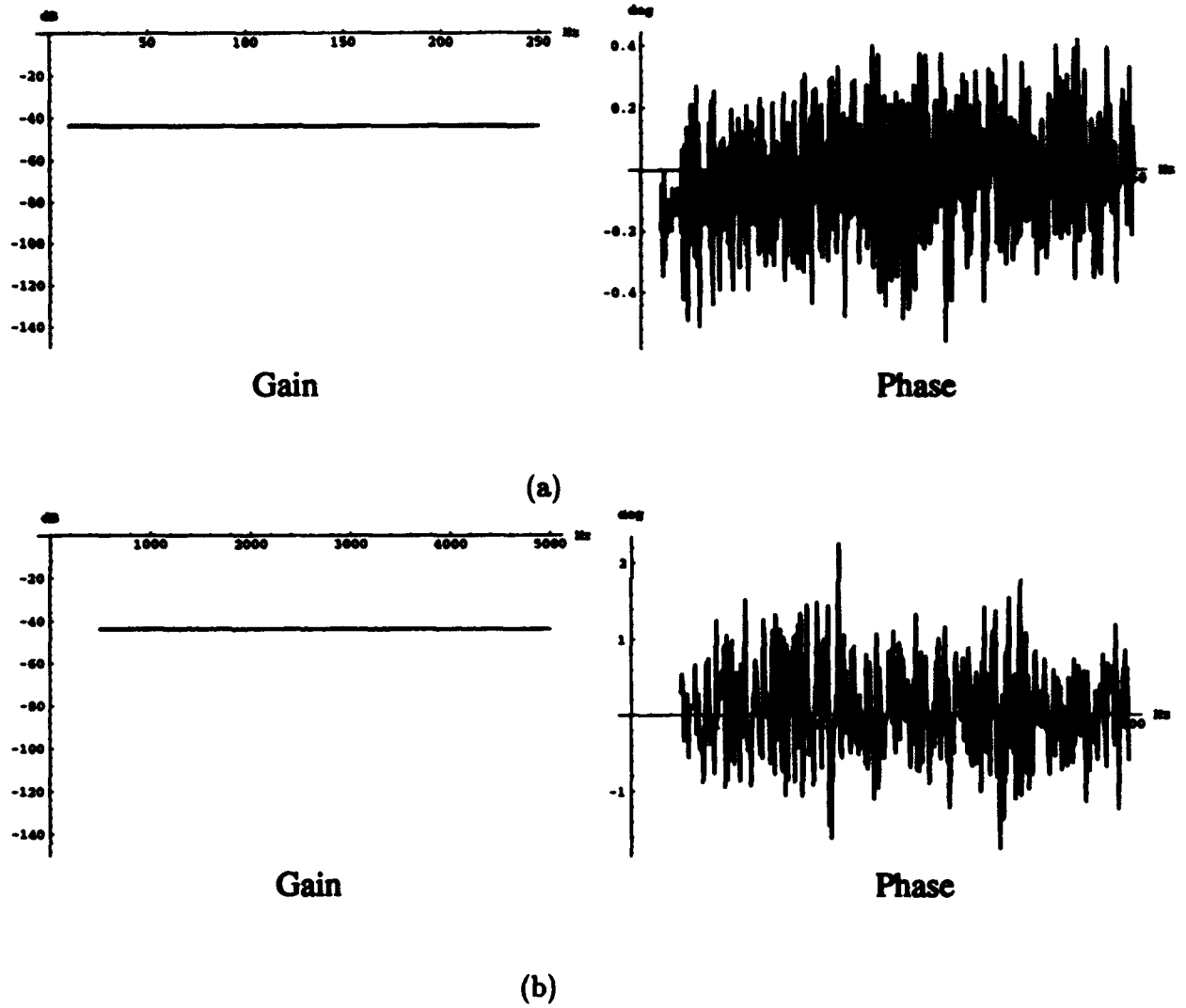


Figure 15. Gain and phase plot for a transfer function from an electrode to the multiplexed output. (a) low frequency signals. (b) higher frequency range.

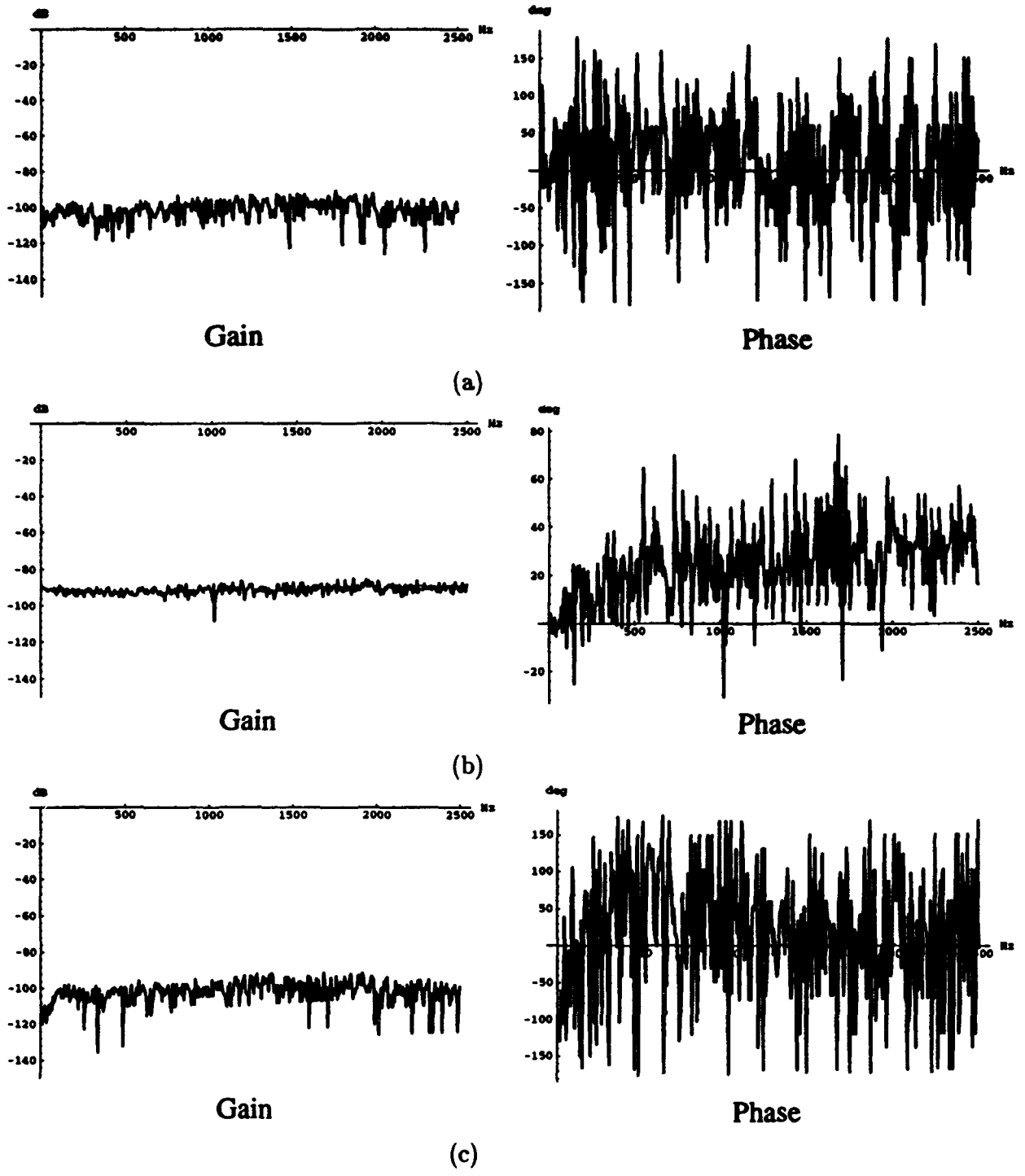


Figure 16. Transfer function from a non-selected electrode to the multiplexed output. (a) for an electrode in the same row as the selected electrode. (b) for an electrode in the same column as the selected electrode. (c) for an electrode in neither the same row nor the same column as the selected electrode.

important to note that measuring the impedance of an open circuit generated a gain of approximately -90 dB to -100 dB, approximately the same range as measured for the non-selected electrodes.

4.3 Conclusion

The fabricated brain chips have now been fully tested. Further, the performance of the individual electrodes has been measured. This verifies that the design of the chips is correct. However, only two of the chips were packaged, and it is thus not possible to test each of the 49 fabricated chips. It is likely that most, if not all, of the chips are functioning.

With the successful design and fabrication of the brain chip, the next obstacle was to develop the methods for applying protective coatings to the non-packaged chips.

V. Encapsulating the AFIT Array

Recall that the brain chip is intended to function resting on the surface of the brain. While on the surface of the brain, the array will be immersed in cerebral spinal fluid (CSF). Also recall that CSF is a fluid containing several alkali ions including sodium (Na^+), potassium (K^+), and chlorine (Cl^-). All of these ions are destructive to active semiconductor devices, however, sodium is the most damaging due to its small size and mobility. Sodium also reacts with the aluminum electrodes causing corrosion of the electrode sites. Therefore, in order for the array to function after implantation in the CSF, it is necessary to provide better passivation than is currently present on the chips.

For reasons discussed in Chapter 2, iridium was chosen to coat the aluminum electrodes, and polyimide was chosen for the passivating coating. However, methods for applying both the iridium coating and the polyimide coatings were needed.

MOSIS returned the fabricated chips in an unpackaged state as is seen in Figure 17. In this unpackaged state, the chip is ready for further processing.

Processing the chips is carried out in two stages. First, the chips are metalized. This stage is done using a standard lift-off technique to pattern the metal. The metalization process is listed in Appendix C. The second stage is coating the array with polyimide. This stage is repeated three times to provide a thick enough coating of polyimide. The process for applying and etching the polyimide is listed in Appendix D. The following sections provide a detailed discussion of the encapsulation procedures.

5.1 Cleaning the Arrays

The first step in any semiconductor processing is to clean the wafers or, in this case, chips. Therefore, a piranha clean was initially performed by immersing the chips in $H_2SO_4 : H_2O_2$ mixed 3:2. Unfortunately, the sulfuric acid reacted with the

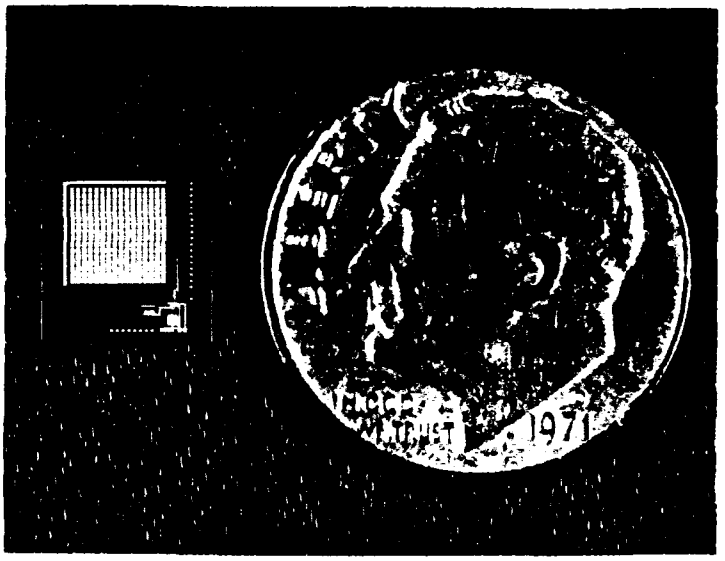


Figure 17. The unpackaged array.

aluminum electrodes. This caused the aluminum to be stripped from the devices and rendered the devices worthless.

A different method was therefore used for cleaning the chips. The clean begins by immersing the chips in an acetone bath for 30 seconds and mechanically agitating the bath. Following the acetone bath, the chips are placed in an ultrasonic bath of methanol for 1 minute. And finally, the chips are removed from the bath, blown dry with N_2, and baked at 200° C for 1 hour to remove any moisture. This process removes any organic contaminants while not damaging the chip. This process is listed in Appendix B.

5.2 Design of the Photolithographic Masks

Encapsulation of the chips requires two separate photolithography steps. Each step uses a unique mask to expose the photo-resist. An AFIT lab, the Cooperative Electronics, Materials, and Processes Laboratory, the co-op lab, has the facilities to manufacture these masks. The process is similar to a standard photographic system,

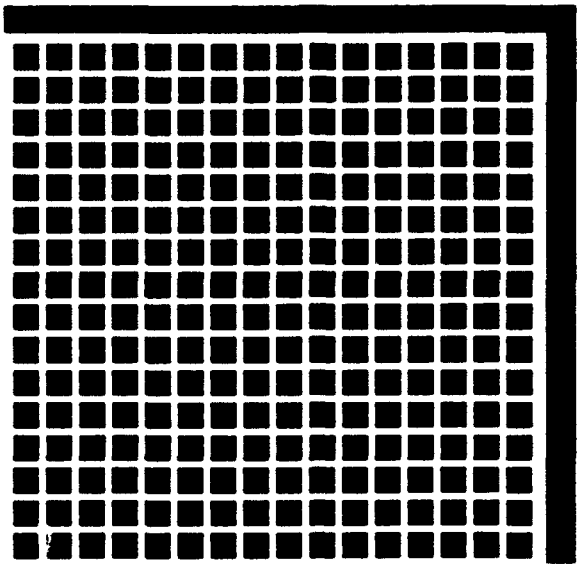


Figure 18. Negative image of the metalization mask.

in which a negative image is projected onto the desired photographic paper. The paper is then developed to bring out the image. However, in producing the masks the image is reduced down onto a photographic glass plate instead of photographic paper.

To begin the process, the desired reduction factor is chosen. For the brain chip, the maximum reduction factor of 50 was selected. After selecting a reduction factor, the mask images were generated using a standard image editing program on the NeXT workstations. Figures 18 and Figure 19 provide pictures of the metalization mask and the polyimide etch mask, respectively. After generating the mask images, the images were printed out on standard transparencies. It was necessary to print two complete copies of each mask. The copies were then overlaid in order to make the image dark enough for a proper exposure of the photographic plates.

Using the negative images, several plates were exposed. Exposure times of 5 to 5.5 minutes were used. The plates were developed by immersion in a developer solution for 2 minutes. This was followed by a stop bath solution for 1 minute. And finally the plates were immersed in a fixer solution for 1-2 minutes.

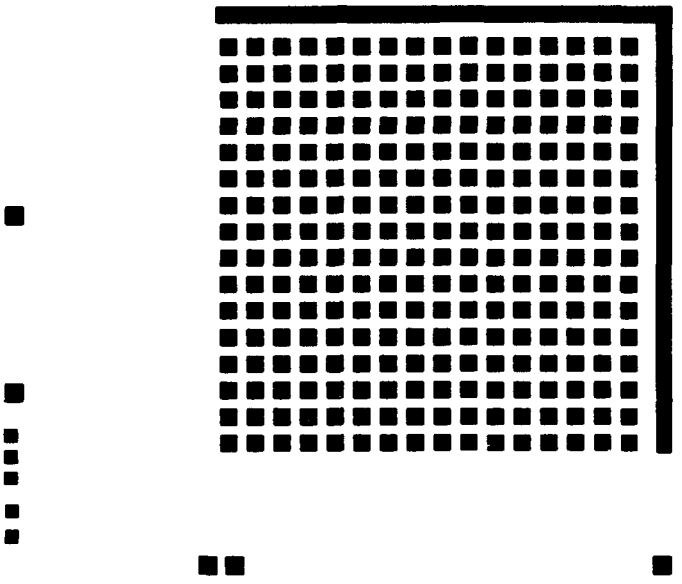


Figure 19. Positive image of the polyimide etch mask.

The metal mask leaves electrode openings that are $200\mu m$ square. This is slightly larger than the actual aluminum electrodes, and allows the iridium coating to extend beyond the physical electrode site. The polyimide mask electrode openings are $150\mu m$ square. This is slightly smaller than the actual electrodes and ensures that polyimide will cover all of the edges of the electrodes. By sizing the masks in this manner, proper protection of the electrode is insured. Figure 20 shows the structure generated by the entire encapsulation process.

The polyimide mask includes several openings for bonding pads. However, openings in the polyimide mask are provided only for certain bonding cites. Therefore, if additional connections are desired, the polyimide mask will need to be redesigned. Also note that the image of the polyimide mask is actually a positive image. Therefore, after the image is printed onto a plate using the reducer, it is necessary to reverse the image using the duplicator.

Unfortunately, the fabricated masks are not exactly the size of the fabricated electrode array. The difference in size is very minor, less than $15\mu m$ across the entire length of electrode array, or less than a $.1\mu m$ difference in the center to center

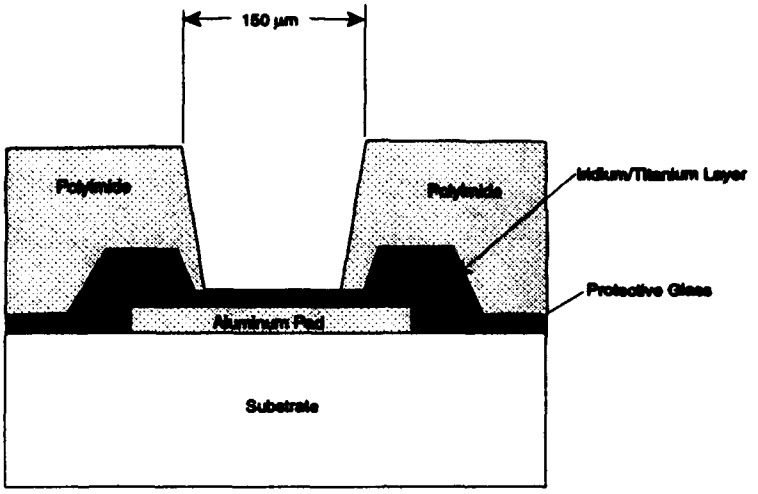


Figure 20. Electrode structure after metalization and application of the polyimide.

spacing of the electrodes. For the metalization mask this caused very little problems, however, for the polyimide mask, it was very difficult to align the mask such that none of the edges of the electrodes are exposed. Further, openings for the power and ground connection are offset by an additional 10 μm. This caused significant difficulties in aligning the mask for the polyimide etch. Fortunately, with each of the successive layers of polyimide, the alignment can be varied slightly to ensure a good coating of the electrode surface. Portions of the power and ground pads were covered with polyimide, but exposed area of the pad was still large enough to permit proper bonding to the pads. For future work, the polyimide mask should be remade. However, it is important to note that the masks can be successfully used. It is currently unknown why the masks were scaled slightly wrong. The most likely explanations are that either the output from the image editing program to the printer was slightly off scale, or that the reduction factor was not exactly 50. The power and ground connections are misplaced in the original image used for making the mask.

5.3 Electrode Coating

Iridium was chosen as a protective electrode coating due to its inert nature, however, because of its inert nature iridium does not adhere to most surfaces. Therefore, titanium is used as a "glue" layer in between the aluminum electrodes and the iridium coating. Titanium is known to be highly reactive and therefore adheres well to most other metals including both aluminum and iridium. Deposition of the metals was performed using the Denton DV-602 RF sputtering system located at the co-op lab.

To deposit the metals, titanium is first deposited, and then without removing the chips from a vacuum the iridium is deposited. This method must be followed due to the highly reactive nature of the titanium. If the deposited titanium were removed from the vacuum, it would oxidize forming titanium dioxide to which iridium does not adhere.

Metal thicknesses of approximately 300 Å for titanium and 3000 Å for iridium were desired. Therefore, deposition rates for both metals had to be determined.

5.3.1 Measuring Deposition Rates. The rate at which a metal is sputtered is dependent upon the factors listed below.

1. Metal
2. Vacuum pressure during deposition
3. Power being applied through the circuit (forward power)
4. Power reflected by the circuit

During a sputtering session, vacuum pressure is dependent on the flow of the ambient argon gas. The flow of argon gas also affects the percentage of power that is reflected by the circuit. Further, the metal used will affect the reflected power. Due to these inter-dependencies, all parameters can be determined by the metal, the forward power, and the argon gas pressure. Also note that each sputtering session will vary

Table 3. Sputtering deposition rates for titanium. Note that there was a significant amount of variance in measuring the metal thickness. Therefore, all values are approximate.

Forward Power	Pressure (μm)	*Time (min.)*	*Thickness* Å	*Rate* $\left(\frac{\text{Å}}{\text{min.}}\right)$
350	1.4	20 min	500	25
150	1.5	25 min	400	16
150	1.4	20 min	300	15

Table 4. Sputtering deposition rates for iridium.

Forward Power	*Pressure* (μm)	*Time (min)*	*Thickness* Å	*Rate* $\left(\frac{\text{Å}}{\text{min.}}\right)$
350	1.3	20 min	2000	100
200	1.3	20 min	1000	50
200	1.3	45 min	2300	51.1
200	1.3	50 min	2500	50

from the standard values. This variance was typically small and should not greatly affect the thickness of the deposited metal.

In general, the less power applied to the circuit and the lower the vacuum pressure, the slower the deposition rate will be and the more uniform the metal coating will be.

Table 3 shows the deposition rates measured for titanium. Table 4 shows the deposition rates measured for iridium. Thickness measurements were taken using a Dektak IIA profile measuring system. The Dektak measurements taken of titanium thickness are not highly accurate due to the thinness of titanium layer that was deposited. However, titanium was needed only to get the iridium to adhere to the test silicon wafers, and later the aluminum electrodes. Therefore, after successfully sputtering iridium onto a titanium coated wafer, it was clear that the titanium layer was sufficiently thick. Measurements of the iridium's thickness were taken on dual layers of iridium and titanium. This was necessary because previous tests showed that iridium would not adhere to a silicon wafer.

Table 5. Selected values for metal deposition.

Metal	*Forward Power*	*Pressure (μm)*	*Time (min)*	*Thickness Å*
Titanium	150	1.4-1.5	20	300
Iridium	200	1.3-1.4	50	2500

The final parameters selected are shown in Table 5. The sputtering times were increased during the later runs to increase the thickness of the iridium layer. In these later runs the iridium was sputtered for 75 minutes instead of 50, thus increasing the thickness from about 2500 Å to about 3800 Å.

After determining the parameters for sputtering the metal, a positive photolithography process was used to pattern the metal.

5.3.2 Lift-Off Process. The positive photolithographic process used is a standard process. The first step is to apply the adhesion promoter hexamethyl disilazine, HMDS. This is done by puddling HMDS onto the chip and then spinning at 4000 RPM for 45 seconds. Immediately after applying the adhesion promoter, the positive photo-resist, Shipley AZ1350J, is puddled onto the chip and spun at 5000 RPM for 45 seconds.

The resist is hardened by a soft bake at 70° C for 20 minutes. The length and heat of the soft bake affect the length of the exposure time necessary. However, the values used for the soft bake were standard values.

The resist is exposed using high intensity ultraviolet light. The metalization mask was used to pattern the resist. For positive photo-resist, the exposed areas are removed during development. The time of the exposure is very important. Improper exposure will cause edges to lose definition and corners to be rounded. Using test silicon wafers various exposure times were tried in order to determine the proper length. Table 6 shows the results for various exposure times. However, exposure time varies with the surface under the resist. This proved to be a factor in switching the process from silicon wafers to the actual brain chips. This difference caused the

Table 6. Positive photo-resist exposure times.

Exposure Time (sec.)	*Pattern Description*
30	Edges poorly defined.
50	Pattern appears good, but some edges appear to be poorly defined
60	Pattern appears excellent
75	Pattern appears excellent
90	Corners are distinctly rounded, definite over exposure

exposure time used with the brain chip to be decreased from 65-70 seconds to 58-62 seconds.

After exposing the resist, the chips were soaked in chlorobenzene for 2 minutes which causes the positive photo-resist to swell. A second bake at 90° C for 15 minutes is used to harden the resist.

The resist is developed using Shipley AZ351 positive photo-resist developer mixed 1:3 with de-ionized water (DIW). To apply the developer, the target is spun at a rate of 1000 RPM while the developer is sprayed onto the target for 45 seconds. This is immediately followed by spraying the target with DIW for 30 seconds. Finally, the chip is blown dry with N_2. The resist is then examined to ensure that the pattern is well defined. If the resist is not completely developed, then the developer can be sprayed onto the chip for an additional amount of time. A final hard bake at 90° for 15 minutes solidifies the pattern.

The chips are now taken to the sputtering system and the metal is deposited. Note that after the photo-resist is applied, the metal deposition should proceed within a matter of hours.

After the metal is deposited, the chips are soaked in acetone. The acetone dissolves the remaining photo-resist. This removes the base from under the undesired metal causing it to be lifted off of the target. Unfortunately, the process generally

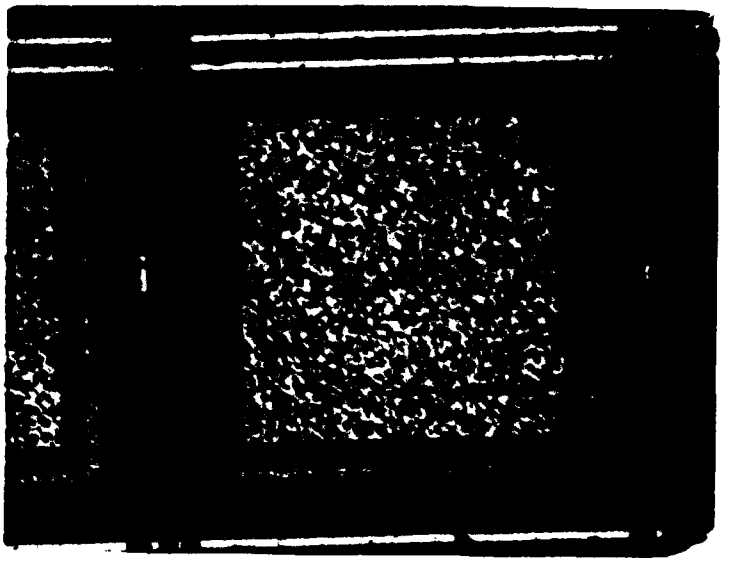


Figure 21. Typical electrode site following metalization.

does not lift off all the metal easily. Therefore, it is necessary to scrub the chips gently with a cotton swab.

5.3.3 Sticky Tape Test. After depositing the metal, the 'sticky tape test' was employed to ensure that the iridium had adhered to the electrodes. The test is performed by pressing one of the chips onto scotch tape, and then pulling the tape off. If any of the metal is removed by the tape, the device fails the test. Using the titanium iridium layer, the device passed the sticky tape test. Further, testing was done by attempting to scratch the iridium coating with a metal object. While this method did damage the surrounding glass coating and several other structures on the chip, the electrode coating remained unscathed.

5.3.4 Results of the Electrode Coating. Figure 21 shows a typical electrode site. As can be seen, the electrode itself is well covered. However, around the edges of the electrode it is clear that the titanium-iridium coating did not adhere to the protective glass. This causes the edge of the electrode to appear rough and poorly

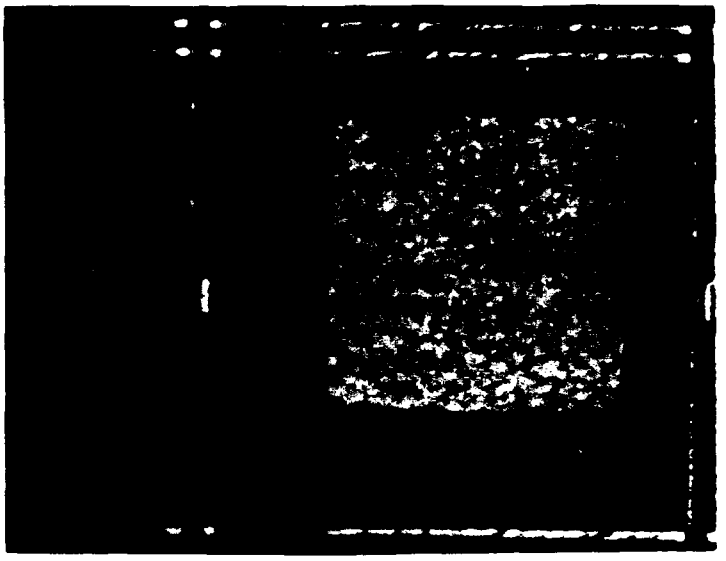


Figure 22. Typical electrode site following metalization and encapsulation with polyimide.

coated. However, the actual aluminum is fully coated, and the polyimide passivation leaves only the coated portion of the electrode exposed as seen in Figure 22.

With most of the chips that were metalized, 1 or 2 of the electrodes came out with poor coatings. An example of this is provided in Figure 23. As can be seen, the iridium coating has left a portion of the aluminum electrode exposed. In some cases, the exposed aluminum is on the side of the electrode and is therefore covered by the polyimide. The holes in the electrode coating were most likely caused by contamination, such as dust, during the photolithography processing. Therefore, in order to reduce the number of bad electrodes, it is essential to blow the chips with N_2 before each of the processing steps.

5.4 Applying the Polyimide

As with the work done by Denton and Hensley, and later Ricardo Turner, the polyimide used here is DuPont Pyralin PI-2555. Ricardo Turner developed a method

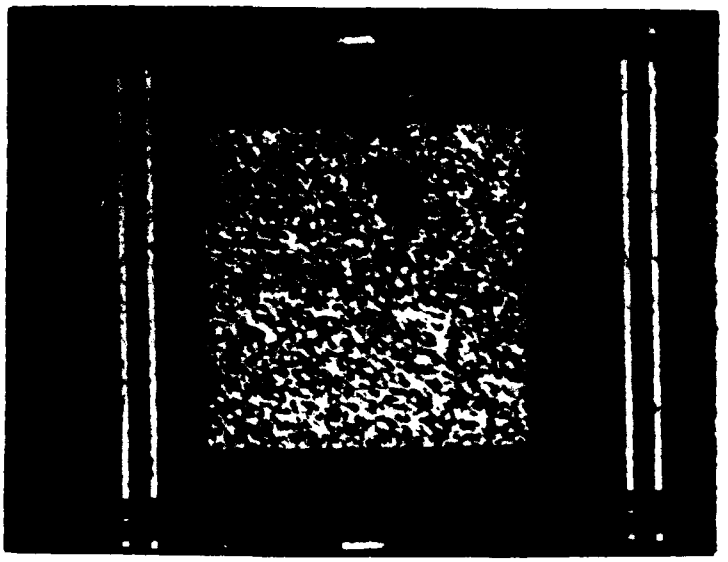


Figure 23. Electrode with holes in the iridium coating.

for applying the polyimide to the chips (30:III-1-12). His process with a negative photo-resist has been modified and used here. However, due to availability, the type of photo-resist has been changed to Waycoat HR-200.

The general process begins with the application of the polyimide. On top of this coating, a negative photo-resist is applied. The photo-resist is exposed with the desired pattern, and then developed. Positive photo-resist developer (Shipley AZ351) is then used to etch the polyimide. The polyimide is then cured. And finally the photo-resist is removed. The entire process is repeated three times to generate a thick coating of polyimide. Turner spun the polyimide on at a faster rate and used 4 separate coatings to apply the polyimide (30:III.3). However, etch times required for the fourth coating were found to cause significant under cutting. Therefore, it was decided that three coatings were sufficient. Note that German suggested that greater than 10 kÅ be applied (9), and with this process over 75 kÅ are applied.

5.4.1 Application of the Polyimide. First, the chip is cleaned using the method listed in Appendix B. Next, the chip is blown off with N_2 to remove any surface dust and an adhesion promoter is applied to the chip. For DuPont Pyralin PI-2555, DuPont recommends using their adhesion promoter VM-651. The VM-651 is mixed in a solution of 95% methanol, 5% DIW, and 0.1% (1 drop) VM-651. The mixed solution needs 12 hours to normalize and should not be used more than 20 days after it was originally mixed. La Voie has shown that the use of VM-651 improves adhesion and reduces the number of pin-hole defects in the polyimide coating (23:61-67). Therefore, it is very important that the adhesion promoter be used. The adhesion promoter is puddled onto the chip and then spun at 5000 RPM for 45 seconds.

Immediately after applying the adhesion promoter, the polyimide is puddled onto the chip. Polyimide initially comes as a polyamic acid solution that is converted to polyimide through heat (7). When applied, the polyimide must cover the entire chip, including the edges and corners. This will decrease any edge effects and allow the polyimide to form a uniform coating covering the entire chip. The chip is then spun at 4000 RPM for 45 seconds.

After spinning the chip, the polyimide is soft baked for 20 minutes at 70° C.

5.4.2 Negative Photo-resist Process. A negative photo-resist is used to provide a mask for etching the polyimide. Therefore, negative resist, Waycoat HR-200, is puddled onto the chips. The chips are then spun at 5000 RPM for 45 seconds. The resist is then soft baked at 70° C for 25 minutes. Typically, the resist used is baked at 65° C for 15-20 minutes. However, during exposure, several of the chips were sticking to the exposure mask. Increasing the time for the soft bake reduced this problem, although not completely solving it.

After the soft bake, the chips were exposed with high intensity ultraviolet light. The polyimide mask was used to pattern the photo-resist. With negative

Table 7. Negative photo-resist exposure times.

Exposure Time (min.)	*Pattern Description*
0.5	Pattern is poorly defined
1	Pattern is acceptable but not great
1.5	Pattern appears good
2	Pattern appears nearly perfect

photo-resist, any area that is exposed to light will be hardened and will remain after developing. Development times vary with several factors, and therefore it was necessary to experiment with several different times until an acceptable exposure time was found. Table 7 shows the results for several exposure times using silicon wafers that were coated with photo-resist only. After adding polyimide to the wafers, exposure times needed to be increased from 2 minutes to 3.5 minutes. The exposure time used with the chips was increased again to 4.5 minutes.

Following exposure, the chips are developed by spinning the chips at 1000 RPM and spraying on xylene for 30 seconds followed by butyl acetate for 30 seconds. The pattern is then examined to ensure that it is fully developed, and all edges are well defined. Note that unlike positive photo-resist, if the development of the resist is not complete, both the resist and the polyimide must be stripped off and the entire process repeated.

5.4.3 Polyimide Etch. The polyimide was etched using the positive photo-resist developer, Shipley AZ351, mixed 1:5 with DIW. The developer etches the polyimide very quickly. Various etch times are shown in Table 8. However, the etch time is dependent on the thickness of the polyimide. With the application of multiple layers of polyimide, the thickness that is being etched increases therefore, the first layer is etched for 3.5 seconds, the second coating of polyimide is etched for 5 seconds, and the final layer is etched for 7 seconds. It is important to note here that it is best to err on the side of caution. If the etch is not complete, the polyimide

Table 8. Polyimide etch times.

Etch Time (sec.)	*Etch quality*
3	Etch looks good.
4	Looks great.
8	Appears to be minor under cutting and rounding of the corners
10	Significant under cutting and rounding of corners.
15	Corners are very rounded and extreme under cutting

can be etched for an additional amount of time. However, there is no way to replace polyimide that has been removed except through the application of another coating.

5.4.4 Final Cure. After etching the polyimide, the chip is ready for a final cure. Recall that the polyimide initially is applied as a polyamic acid solution. The final cure will complete the conversion into polyimide. DuPont recommends cure times of 30 minutes to 1 hour with temperatures around 350° C (7). However, due to the active devices on the brain chip, a lower temperature was used for the final cure. Therefore, the cure times were increased significantly in order to ensure a complete cure. Ricardo Turner used 150° C for 2 hours followed by a second cure at 180° for 2 more hours (30:A.8). These cure times were found to be adequate. However, the cure has been changed to a 4 hour cure at 180° C. This cure time can be extended as additional curing does not damage the polyimide coating, however, shortening the cure time could result in an incomplete cure.

5.4.5 Removal of the Photo-resist. After the final cure, the polyimide is resistant to acetone. Therefore, the chips are soaked in an acetone bath and gently scrubbed using a cotton swab. This removes the photo-resist without damaging the polyimide. Turner suggests doing 150° C cure for 2 hours and then removing the photo-resist, and then performing a second cure (30:A.8). However, experiments showed that the HR-200 photoresist was easier to remove if the final cure were completed before stripping the photo-resist.

5.4.6 Results of the Polyimide Cure. In general, the application of the polyimide went very well. However, as has been mentioned, during exposure of the photo-resist, the chips had a tendency to stick to the exposure mask. In order to overcome this problem, the soft bake time for the photo-resist was increased. Further, during alignment, the chips were not brought into full contact with the mask until they were nearly in alignment. Therefore, only minor adjustments were made after the chips were brought into contact.

Some alignment problems were caused by the incorrect scaling of the polyimide mask. It was particularly difficult to align the mask allowing the power and ground contacts to be fully exposed while at the same time the electrode array was properly aligned. Therefore, it was necessary to cover a portion of the power and ground contacts with polyimide. However, the contacts are large enough that bonding to the pads was still possible.

VI. Design of the Implantable Package

In their thesis, Denton and Hensley recommended ways that the implantable package for the array should be redesigned (13:95-97). Therefore, Ricardo Turner designed a new implantable system that allowed the array to be chronically implanted and removed from the subject without surgery (30:Ch. II). Turner experienced difficulties in connecting the chip to the bonding wires and then adding a final coating of polyimide to the package, preventing his design from reaching implantation. However, Turner's general design is sound. Therefore, Turner's package was modified to provide an implantable package.

6.1 Requirements for the Package

During long term exposure to the cerebral spinal fluid, the brain chip is likely to fail due to permeation of the polyimide coating by the cerebral spinal fluid, CSF. Therefore, an implantable chip support package must be easily inserted and removed without requiring further surgery. However, a chronically implanted mount is necessary to secure the implantable package, and provide access to the brain.

Chronic implantation, however, increases the subjects risk of both trauma and infection. Any trauma to the brain can cause edema or neurosis, and may lead to erroneous readings and permanent injury to the subject (13:81). Therefore, design of the package must minimize the trauma caused by insertion and extraction of the chip. Further, the package must limit the exposure of the cortex to any infection.

The next implant of the brain chip will be done with a rhesus monkey. The skull of a rhesus monkey is fairly small, thus the implantable package must be as small as possible.

Finally, the implantable package will be in contact with the cerebral spinal fluid, CSF. Therefore, the materials used in fabricating the package must be highly inert and must have low toxicity.

Table 9. Summary of the implantable packages requirements.

Requirement	*Reason*
Chronically implantable	Allows experimentation over long periods
Easily inserted and removed	Allows a chip that has failed to be replaced
Biocompatable	Will not react with the CSF and harm the subject
Water Tight	Prevent CSF from leaking out of the cranium, and prevent infection from entering
Small Package	Unaffected by the curvature of the skull
Immovable and Stable	Prevent damage to the package and injury to the subject

Finally, like all primates, a monkey has fingers with which to play with any object protruding from its head. Therefore, the package must not be easily damaged, or allow the monkey to easily injure itself.

Summarized in Table 9 the requirements for the brain chip are designed to provide a package for implanting the brain chip while ensuring that the subject is not harmed.

6.2 Design of the Package

The implantable package is based directly on Turner's design. The design uses a hollow cylindrical mount which is surgically placed into the subject's skull. During experimentation, an implantable package containing the brain chip will be placed into the mount, allowing the brain chip to rest on the surface of the brain. In between experiments, a plug will be placed into the mount and a protective cap screwed on to prevent infection from entering the exposed cortex. All of the pieces were either ordered, or manufactured at the AFIT model shop. The manufactured pieces were made using stainless steel. Originally, the pieces were to be fabricated using polyethelyne, however, experiments showed that polyethylene melted at the temperatures necessary for curing the polyimide. Further, for the thin walls of

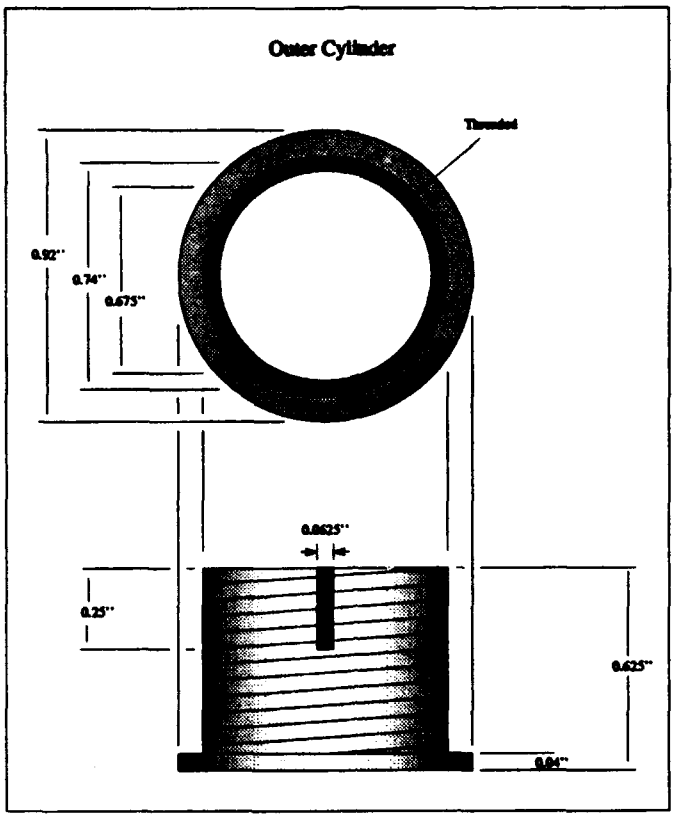


Figure 24. Mount for the brain chip's implantable package.

the mount and the implantable cylinder, the polyethylene did not provide enough structural support causing the pieces to be very pliable.

6.2.1 Mount. As mentioned, the mount consists of a hollow cylindrical structure that will be surgically fitted to the subject. As is seen in Figure 24, the hollow tube has a small flange at the lower end. This flange will rest under the skull and will prevent the mount from being pulled out of the skull. To further secure the mount, a cylinder nut, shown in Figure 25, is screwed onto the cylinder. This nut will be screwed down, sandwiching the skull in between the flange and the nut, thus securing the mount into place. To facilitate turning the nut, two opposing edges of the nut have been flattened. Also in the mount, is a vertical slit, cut through the outer cylinder. This slit is used by the implantation package to prevent the package

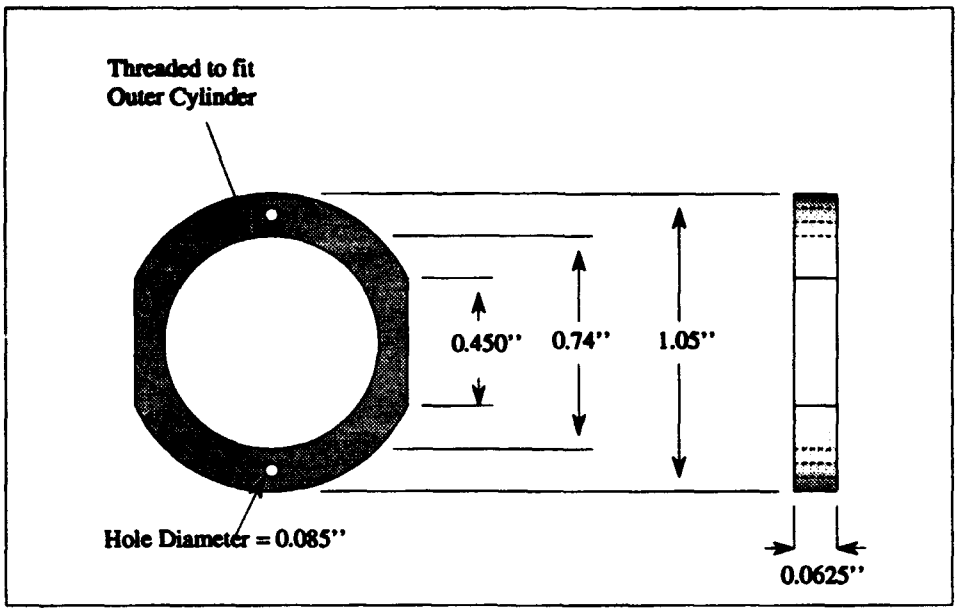


Figure 25. Cylinder nut for securing the mount.

from twisting while it is inside the mount. It also determines the depth to which the implantable package can be inserted. For both the cylinder nut and the protective cap, the outside of the mount is threaded.

6.2.2 Implantable Package. The implantable package consists of two separate parts. First is a hollow cylinder seen in Figure 26 and a cutaway in Figure 27. Second is the header seen in Figure 28. The brain chip is mounted onto the header, as will be described in the next section. The header is then slid into the cylinder and secured in place with epoxy or super glue. Finally, a coating of silicone rubber is applied, covering the bonding pads on the chip, the wire connections from the chip to the header, and connection between the header and the package.

The silicone rubber used on the implantable package will be aquarium sealant. Therefore, it should endure long term exposure to salt water without any leakage. After a 24 hour cure, the sealant is safe for contact with food, and therefore, its toxicity is known to be low. Originally polyimide was to be used for the final coating. However, due to problems discussed in the next section the polyimide was not

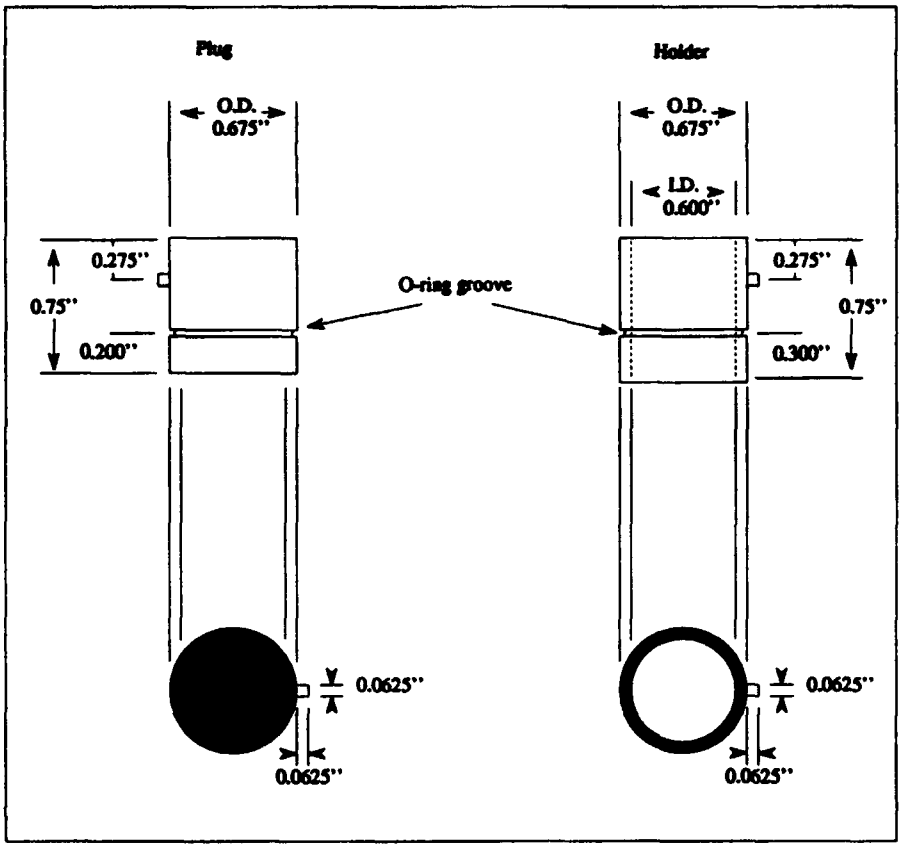


Figure 26. Implantable package cylinder for the brain chip.

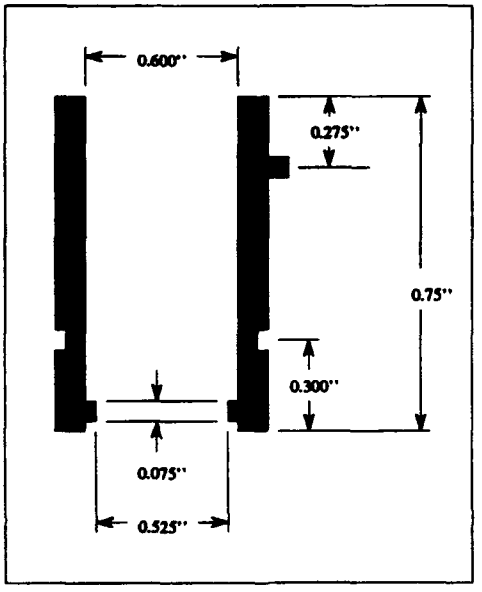


Figure 27. Cutaway of the implantable package cylinder for the brain chip.

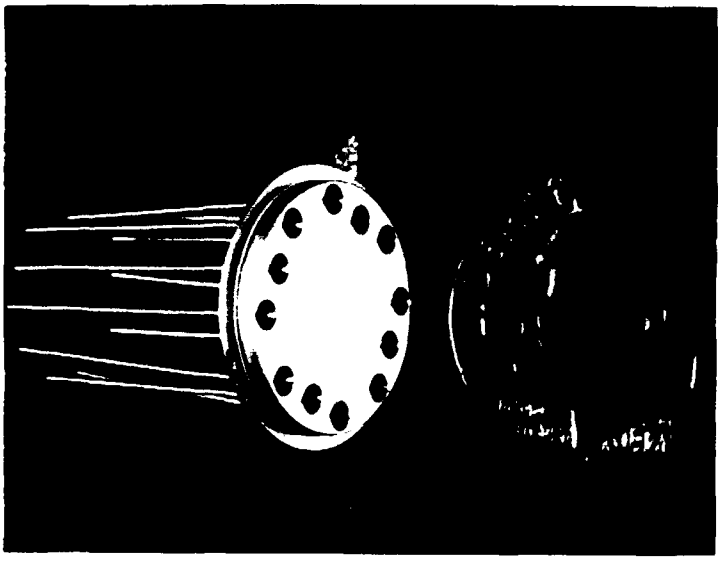


Figure 28. Header package for mounting the brain chip.

adequate for the final coating. However, the silicone rubber appears to be an ideal sealant for the problem.

The hollow cylinder is sized to fit the header exactly. A lip has been added to allow the header to slide down into the cylinder slightly. This makes mounting the header easier, and should aid in providing a better seal. To prevent CSF from leaking out of the skull, an o-ring has been placed around the lower end of the cylinder. This o-ring forms a water tight seal that will prevent any CSF from leaking out of the subjects cranium. Finally, a pin protrudes from one side of the cylinder. This pin slides into the slit of the mount, preventing the cylinder from twisting while situated in the mount.

The header is a microwave device package manufactured by the Airpax corporation. As was seen in the Figure 28, the header has 12 pins. For future work, it would be better to purchase the 16 pin version of this header, allowing the bonding wires to be shortened, and allowing additional connections. Unfortunately, the 16 pin headers were not available when the headers were ordered. For future work the

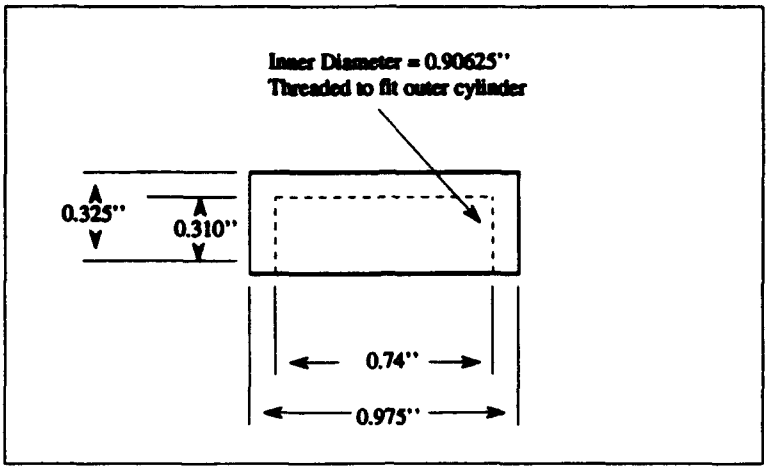


Figure 29. Protective cap for covering the mount.

header size can be reduced from the 0.60 inch diameter header used in this thesis to a 0.50 inch package. This will allow the size of the entire package to be decreased significantly.

6.2.3 The Plug. After the chip has been removed, a specially developed plug will be inserted to prevent any of the CSF from leaking. The plug, shown in Figure 26 is simply a cylinder with a pin and an o-ring. As with the implantable package cylinder, the o-ring forms a seal with the mount preventing the flow of CSF out of the cranium, and preventing infection. The pin servers to prevent the plug from rotating while it is situated inside the mount.

6.2.4 Protective Cap. A protective cap was manufactured to screw onto the top of the mount, enclosing the entire package. This cap should prevent the monkey from accessing the plug and causing himself or the mount physical damage. The cap is shown in Figure 29.

6.2.5 Assembly. For clarity, Figure 30 shows the method of assembly for the entire package.

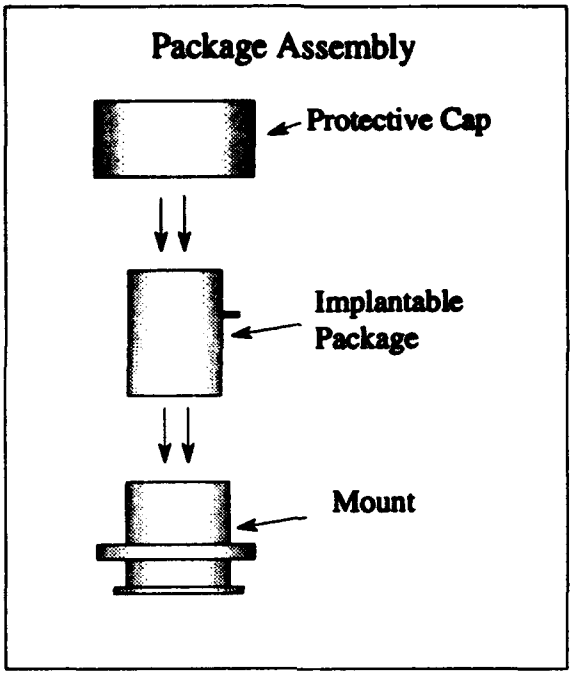


Figure 30. Assembly of the implantation package.

6.3 Interfacing the AFIT Array with the Implantable Package

Turner had several problems interfacing the brain chip with the implantable package (30:III.17-18). The main problem was that during the application of a final coat of polyimide, the bonding wires were pulled off the bonding pads. Turner attributed this problem to the shrinkage of the polyimide as it cools. Another possible cause of the problem may have been that the epoxy the array was mounted in changed its size during the cure. This would cause the chip to move and the bonds to be broken. The TO-8 header provides a more stable mount for the chip, and should prevent this problem. As mentioned, this header is a standard package for use with microwave devices.

Mounting and wire bonding the chip to the header were performed by Larry Callahan at the avionics directorate of Wright laboratories. Appendix E shows the bonding diagram for the implantable package. After the package is mounted and bonded, 2 coats of polyimide are applied to the chip. This polyimide coating is

Table 10. Cure times for final application of polyimide.

Temperature (° C)	*Time (min.)*
70	30
85	30
105	30
130	30
165	360
130	30
105	30
85	30
70	30

applied using a toothpick, and covers all of the bonding pads, and the wires that connect the chip to the header. After the polyimide is applied, the package is cured. However, due to the rate at which the polyimide expands and contracts during the cure, the temperature is raised slowly. Then after the cure, the temperature is gradually reduced. Using this method, no problems were encountered with bonds being destroyed during the polyimide cure. Table 10 lists the times and temperatures used for this final cure.

The polyimide coating successfully covers all of the bonding pads on the chip. Further, it provides a good coating of the bonding wires, and adds physical strength to the wires. Figure 31 shows the array after bonding and the application of 2 coatings of polyimide. However, the initial experiments with the simulated brain showed that contact was being made between the simulated brain and the bonding pins of the header. Using a multimeter to probe the header, it was found that the polyimide had not coated the corners of the header's bonding pins. Therefore, it was determined that the silicone rubber should be used as a final coating to cover the bonding pins. The silicone rubber is also ideal for insulating the connection between the header and the cylinder of the implantable package.

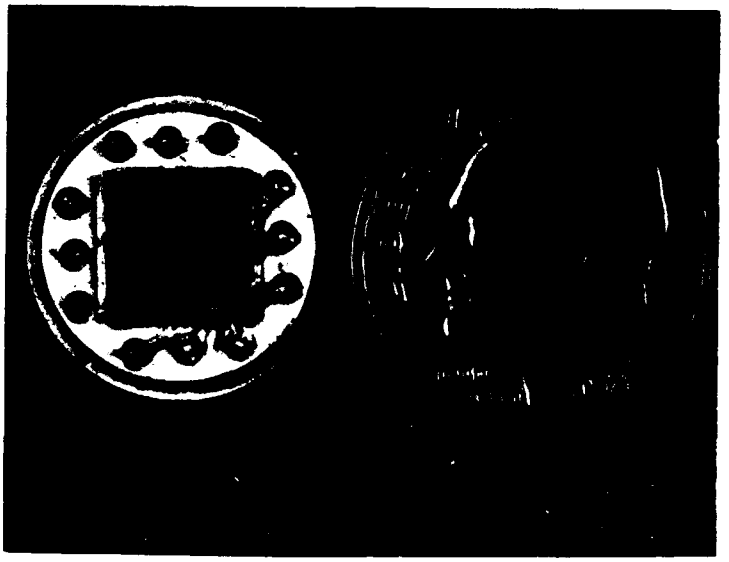


Figure 31. The AFIT array bonded onto the TO-8 header.

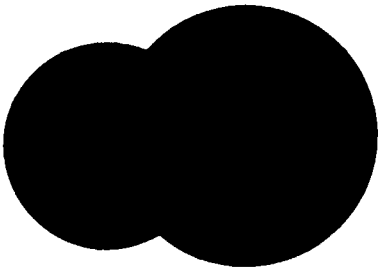


Figure 32. Holes drilled for implantation of the mount.

6.4 Suggested Implantation Procedure

The surgical procedure for inserting the mount is exactly the same as is discussed by Ricardo Turner (30:III.17-20). However, a brief description of the procedure is provided here.

For implanting the device, two adjacent holes will be cut into the skull of the monkey, as seen in Figure 32. The larger hole must be just large enough for the flange to pass through. The smaller hole will be the diameter of the mount cylinder. The mount, with the cylinder nut screwed to a position $\frac{1}{4}$ inch above the flange,

will then be placed into the large hole and moved over to the smaller hole. During this process, the flange should remain below the bone while the cylinder nut remains above. After the mount is in the proper position, the nut will be screwed down tight to lock the mount in place. Bone wax will then be used to seal the large hole. The plug should now be inserted, and the protective cap screwed on.

Finally, to cement the mount in place, dental acrylic will be used. This is similar to the method originally used by Denton and Hensley in their implant (13:78). The bone around the area will be roughed using a dental burr. For added strength, two bone screws will be placed 0.2 inches from the base of the mount. The screws will be on opposite sides and perpendicular to the bone wax. Dental acrylic will then be spread over the entire area, including the mount, bone screws, and bone wax. This will securely cement the mount in place. The skin will then be repositioned around the base of the mount.

The mount is now ready for use. However, the chip should be inserted and removed only when the monkey is restrained. Further, because the monkey is capable of reaching the mount with both its hands and feet, a collar should be placed around its neck. This should prevent the monkey from reaching up and manipulating the implantation package or the associated wires.

6.5 Discussion

As mentioned, a preliminary implantable package was fabricated by the AFIT model shop. However, after examining the fabricated package, several design errors were found. Therefore, the implantation package design should be modified before it is used in an implant. However, the modifications are relatively minor. The primary problem with the new package is that when the implantable package is fully inserted in the mount, removal of the package is difficult due to the short extension of the implantable package beyond the mount. This can be easily fixed by making the cylinder longer allowing it to extend further out from the package. A similar

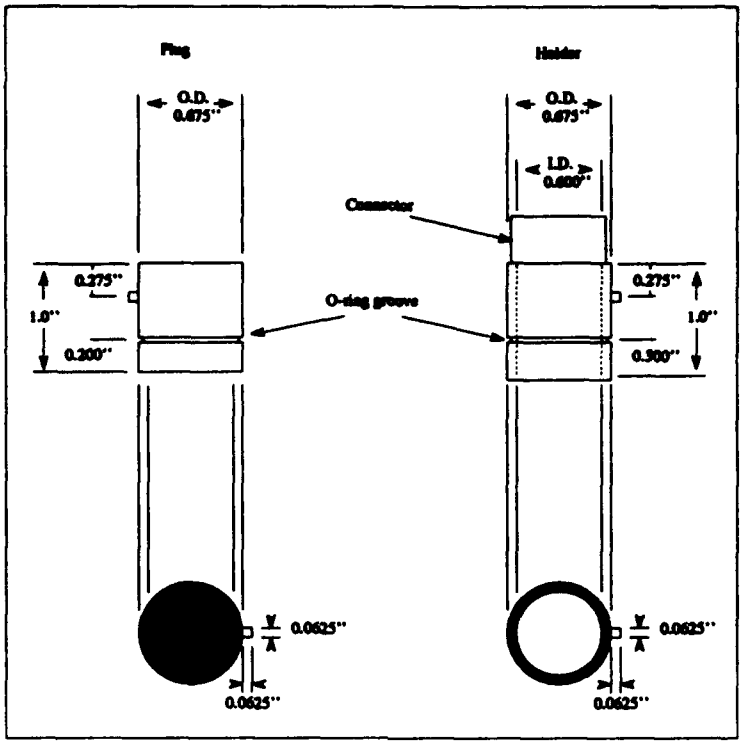


Figure 33. Redesigned implantable package cylinder for the brain chip.

modification will be needed for the plug. Second, the entire system of the mount, the plug, and the protective cap is fairly heavy. Most of the weight is caused by the protective cap and the inner plug. This can also be easily remedied by fabricating the plug and the protective cap out of polyethylene. If possible, it would be best to include a plug connector with the implantable package. This connector would provide a direct interface from the implantable package to any external circuitry. Figure 33 shows the redesigned implantable package cylinder.

The implantable package designed in this thesis is very similar to the package designed by Ricardo Turner (30). However, several important modification have been made. Most notably, the chip is now mounted on the TO-8 header. This provides the chip with a more secure mounting and simplifies the problem of wire bonding the chips. The additional stability of the header allows polyimide coatings to be applied without the wire bonds being pulled up. The header has also allowed

the overall package to be decreased in size by approximately 5%. This design uses silicone rubber as a final sealant. The silicone rubber is capable of providing a thick coating that covers over any sharp edges. This prevents the corners of the chip from scaring the brain, and should help prevent any trauma to the subject. Finally, o-rings have been added to the implantable package to prevent any leakage around the implantable cylinder. This should further reduce the chance of infection. These modifications have improved the implantable package significantly.

Following the methods detailed in this chapter, and Chapter V, several chips were packaged to various degrees. Testing was then done on one of the encapsulated chips.

VII. Testing the Encapsulated Array

Several of the fabricated chips were metalized and encapsulated as discussed in Chapter V. Five of these were mounted onto the TO-8 headers and bonded according to the diagram in Appendix E. During application of the final coating of polyimide, bonding wires were pulled off of two of the arrays due to a slip with the toothpick. Of the remaining three chips, the counter was functioning on two of the devices. One of these two, which had two coatings of polyimide, was chosen for encapsulation with the silicone rubber. This device was tested in a saline solution for several days. Low signal level inputs were recorded from a simulated cortex, thus showing that the array was properly functioning.

7.1 Test Set Up

In order to test the chip, a simulated cortex was fabricated. Driver (Clock, RESET, Power, and Ground) and V_{DD} inputs were connected to the chip, and the signal outputs from the chip were measured. A schematic of the test set up is shown in Figure 34. From the bonding diagram in Appendix E, it is clear that there are 8 I/O connections to the brain chip. Four of these connections are inputs required for the multiplexing circuitry to function; power, ground, clock, and reset. The

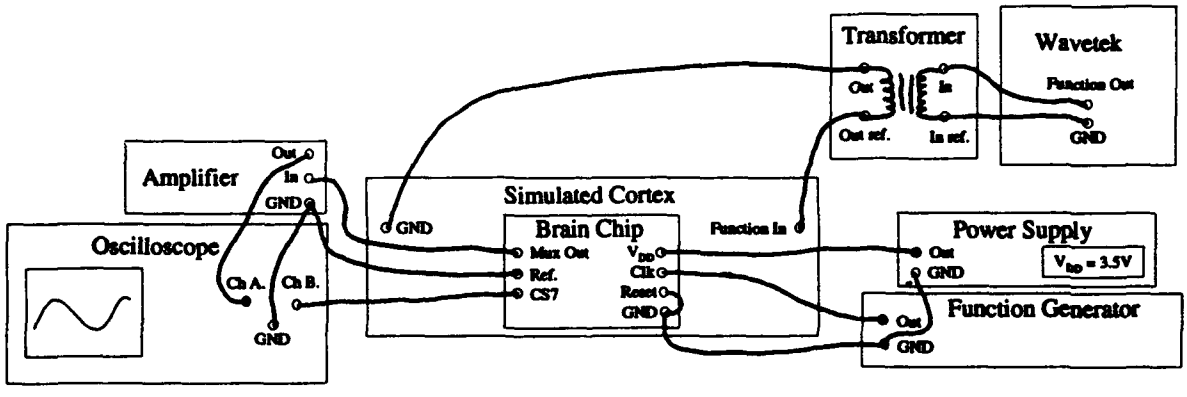


Figure 34. Setup for testing the encapsulated array.

remaining four connections are outputs from the chip; CS7 (the lowest frequency output from the counter), column synch, multiplexed output, and the reference. During testing, a sinusoidal signal was applied to the simulated cortex. The brain chip was then pressed onto the saline saturated paper towel and the potential between the reference pad and the multiplexed output was recorded.

7.1.1 The Simulated Cortex. The simulated cortex consists of a paper towel that was neatly folded to form a rectangle of approximately $7cm \times 20cm$. The towel was soaked in a 0.9% saline solution, which approximates the saline content in the cerebral spinal fluid. Recall that sodium is the most damaging of the alkali ions. Therefore, it was assumed that permeation of the protective coating by sodium would occur before permeation by other alkali ions. And thus, testing with sodium sufficiently approximates the neural environment.

In order to provide an input signal, a Wavetek function generator was connected to an isolation transformer. The output leads from the isolation transformer were then connected to opposite ends of the paper towel. This generates a varying voltage potential across the towel.

The Wavetek was set to generate a sinusoidal function of varying frequency and amplitude. Note that the peak-to-peak value of the input sine wave will not be the peak-to-peak value of the measured signal. Indeed, the measured signal will depend on the the location of the reference and the location of the measuring electrode. The ideal goal of this testing is to pick up a voltage potential in between the reference electrode and the individual electrodes.

7.1.2 Power Supply. The power supply used was a standard HP power supply. The power supply provided a constant measure of both supply voltage and current. The ground of the power supply was common with the ground of the pulse generator used to provide a clock input. To begin testing, an input voltage, V_{DD}, of 5 volts was used. However, for later testing V_{DD} was lowered to 3.5 volts.

7.1.3 Clock Input. The clock was generated by a pulse generator. The clock input was a 50% duty cycle square wave with a peak-to-peak voltage equal to V_{DD}. The clocks frequency varied during testing, but was generally set to 256 kHz. At this frequency, each electrode is sampled 500 times per second.

7.1.4 Measuring the outputs. To monitor the outputs from the chip, a standard oscilloscope with two, 1 $M\Omega$ impedance, input channels was utilized. During testing, the column synch was not monitored. This signal is redundant, and was connected only to verify that the decoder was functioning. Therefore, the potential between ground and the brain chips counter was measured with one channel, and the potential between the reference pad and the multiplexed output was measured with the other. However, in order to properly test the brain chip, the measurement of signals with peak-to-peak voltages less than 1 mV was desired. Most oscilloscopes, however, require that input signals have peak-to-peak voltages greater than 5 mV. Therefore, a Stanford Research, low noise amplifier was used to amplify the signal from the multiplexed output.

The amplifier is capable of amplifying signals by a factor of up to 50,000. Typical signals recorded by Denton and Hensley had peak-to-peak voltages of 500 μm to 1 mV. Therefore, amplification of the signals by a factor of 100 to 200 is desired. This will bring the peak-to-peak potentials above 50 mV, well within the range of the oscilloscopes.

The amplifier also brings the added capability to filter the incoming signal. The amplifier can apply low-pass, high pass, or band pass filters to the signal, with roll off of 6 or 12 dB per octave. During testing, a high pass filter with a 12 dB per octave roll off, beginning at 3000 Hz, was typically used. This was done to filter out low frequency noise picked up by the wire connecting the chip to the amplifier.

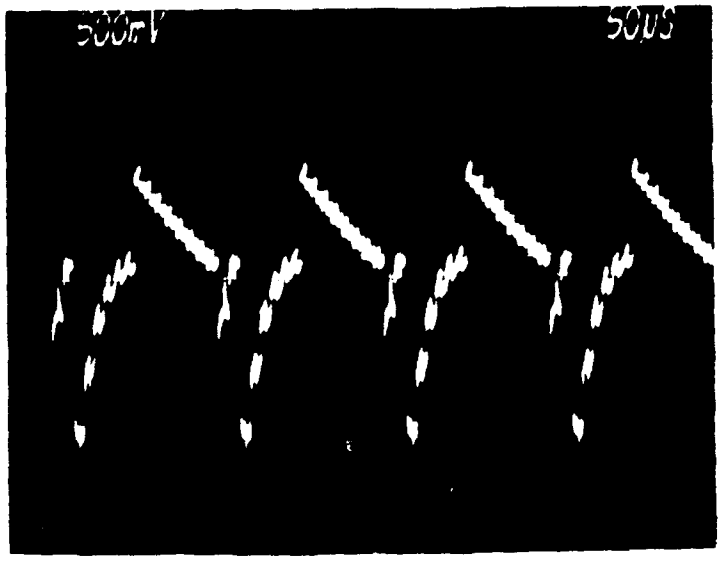


Figure 35. Clock noise on the multiplexed output. The amplifier gain is set to 500. The peak-to-peak voltage of the noise is approximately 5 mV. Note that no input signal is being applied to the electrode array.

7.2 Testing Results

7.2.1 Clock Noise. The first notable result of testing was that the clock was significantly affecting the output channel. As can be seen in Figure 35, clock noise is on the order of 20 mV. However, this noise was collected while the output from the chip was directly connected to the input of the amplifier. The amplifier, has an input impedance of 100 $M\Omega$, therefore, it was believed that much of the noise was caused by capacitive coupling. To decrease this problem, a shunt resistor was placed in parallel with the multiplexed output and the reference pad. Placing the resistor in the circuit gives the capacitor an output path to discharge, thereby reducing the noise. Resistors of several values were tried with good success indicating this is not a critical parameter. The effect of a 2.1 $k\Omega$ resistor is shown in Figure 36. However, placing a resistor in the circuit also creates a voltage divider with the electrode

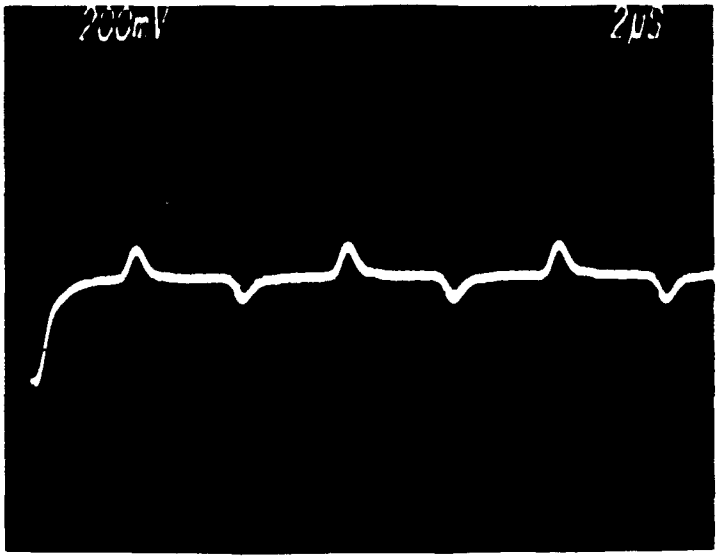


Figure 36. Reduced clock noise. Amplifier gain is set to 100. The peak-to-peak voltage of the signal is approximately 4 mV. No input signal is being applied to the electrode array.

impedance, and the resistor. Therefore, the lower the resistance, the lower the value of the measured signal. Also, this increases the signal to noise ratio to useful values.

Recall from Section 4.2 that the internal characteristic impedance of the circuit was approximately 3.6 $k\Omega$. The value used for the shunt resistor should be guided by the magnitude of the circuits impedance to prevent excessive loss of signal.

In order to measure the impedance of the electrode array while the multiplexor was functioning, a signal was propagated through the array. The amplitude of the input signal was adjusted until the measured signal had a peak-to-peak voltage of 40 mV. Resistors of varying values were then tested. For a resistance of 2.1 $k\Omega$ the measure peak-to-peak voltage was approximately 22 mV. Therefore, the impedance of the circuit is approximately 2.0 kΩ. This raises the question of why this value is significantly less than the previously measured value of 3.6 $k\Omega$. However, recall that impedance decreases with frequency. In measuring the initial value a single

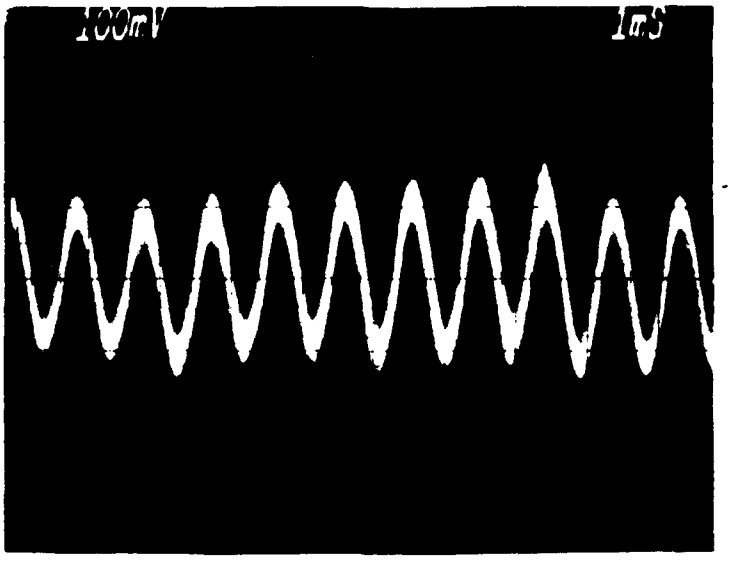


Figure 37. Signal being measured through the array. $R_{SH} = 2.1k\Omega$. Gain = 20. Measured signal has a peak-to-peak value of 15 mV.

electrode was used. In measuring the second value, the electrodes were sampling an input signal. Therefore, the circuit is operating at the frequency of the clock, and the impedance should be lower. Further, note that the original value is only approximate, as is the measured value of 2.1 $k\Omega$. And finally, consider that device characteristics will vary with each individual chip. This variance should be relatively small, but will provide some difference in the electrodes impedance.

7.2.2 Recorded Signals. In order to test the chip, an input sine wave was driven across through the towel. During testing, sine waves of varying frequency and amplitude were measured with the brain chip. As shown in Figure 37, signals with measured peak-to-peak voltages of greater than 15 mV were measured fairly clean. However, lower level signals have significantly more noise as shown in Figure 38. Keep in mind that these signals were measured with a shunt resistor of 2.1 $k\Omega$.

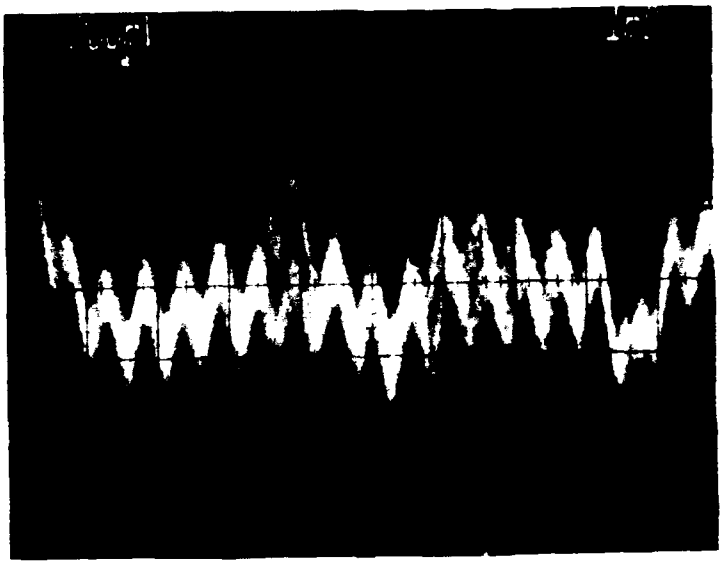


Figure 38. Signal being measured through the array. $R_{SH} = 2.1k\Omega$. Gain = 100. Measured signal has a peak-to-peak voltage of 3.5 mV.

Therefore, the actual potential from the electrode to the reference is approximately 1.8 times larger than the values recorded here.

The noise in the circuit may cause some problems with recording neural signals. However, the majority of the measured noise was generated by the clock. This noise is both periodic and predictable. Therefore, it is possible to sample the data only when the clock noise is near zero, thus reducing its effect on the output signal. Recall that, as shown in Figure 36, during the flat periods, the noise from the clock is minimal. Sampling during these periods should produce very clean signals.

Finally, in order to ensure that the signal was propagating through the electrode array, the input clock and V_{DD} were set to 0. While in this state, all electrodes should be cutoff, and no signal should propagate through the system. As expected, the measured signal was no longer present.

7.2.3 Checking Individual Electrodes. After ensuring that signals were propagating through the packaged brain chip, the next step was to determine if all of the electrodes were functioning. Therefore, using a Micromanipulator microprobe system, sinusoidal inputs were placed onto electrodes individually. During this testing, it was found that only the electrodes in the first column were functioning. The most likely cause for this was that the column decoder was no longer functioning. Examining the output from the column decoder verified that it was no longer functioning.

It is possible that sodium ions managed to permeate the polyimide coating and cause the decoder to fail. At the time that the decoder failure was discovered, the chip had undergone testing on three separate days. Each day the chip was subject to testing in a 0.9% saline solution for several hours. Further, after testing the chip was removed from the saline, but not washed off. Therefore, a layer of salt was left on the chip for the entire time. However, no other circuitry had failed at this point, including all 16 of the electrodes in the first column. As polyimide covers the decoder and the surrounding area for over 100 μm, it seems likely that the electrodes would fail before the decoder.

A more likely explanation for the decoder failure is static discharge. During testing, the package was often handled without proper static protection. Of the 8 connections that were bonded to the package, the decoder, the counter, reference, and the multiplexed output, do not have static protection. However, the reference pad is connected to no active devices, and therefore is highly unlikely to fail. This leaves three connections that static charge could affect. Due to the small size of the transistors, CMOS circuits are very sensitive to static discharge. It is highly likely that static charge damaged the decoder during handling. Although it is surprising that both the counter and the multiplexed output were functioning, it is possible that the design of the decoder is more sensitive to static discharge.

A final possibility is that there was a fabrication error in this particular chip. While both of the MOSIS packaged chips functioned, it is likely that some of the 49 chips received did not fully function. In the future, the output from the decoder should be removed as the connection provides no useful information. Further, the outputs from the counter should be connected to pads with proper static protection.

7.2.4 Endurance Testing. Time constraints did not permit properly testing the life time of the package. Testing was done on the first chip intermittently over a period of 8 days. The longest test ran overnight for 12 hours, during which the counter was continually running. At the end of the test, there was no noticeable change in the output signal from the chip.

After testing was completed, the chip was removed from the saline solution and allowed to dry. However, when the water evaporated, a layer of sodium was left behind. 7 days later, the device was tested again and the counter was no longer functioning properly. This failure can only be due to the permeation of sodium. The chip was examined under a microscope and appeared to be in good shape. However, sodium deposits could be seen covering the entire chip. Therefore, the entire package was soaked in de-ionized water and blown dry with N_2. This process was repeated several times to remove the sodium coating.

After the process was repeated several times, several large cavities appeared on the surface of the chip. In particular, holes appeared in several of the electrodes, and in the polyimide layer as seen in Figure 39. It seems likely that sodium was able to permeate the electrode and corrode the aluminum at these sites. However, a large portion of polyimide was also removed. The area uncovered by the polyimide exposed the entire column decoder as seen in Figure 40. This opens the possibility that sodium did manage to reach the decoder causing it to cease functioning early in testing. What caused the polyimide to be weak in this area is currently unknown.

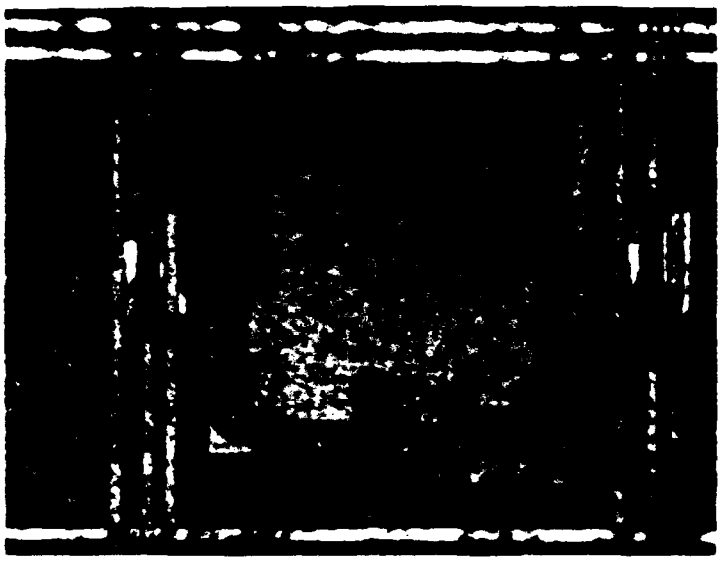


Figure 39. Holes found in the electrodes after testing.

Figure 40. Hole in the polyimide coating after testing.

From the examination of the chip, it is clear that sodium was penetrating the device, although at a very slow rate. This testing suggests that the brain chip should be able to function for a minimum of 24 hours *in vivo*. However, the chip should be expected to function for a period of a week. Currently, a second chip has been coated with silicone rubber and is ready to begin testing immediately. The results of this test will provide more information of the expected life of the chips.

7.3 Discussion

One of the AFIT arrays has been successfully packaged and tested in a saline solution. The array was able to record low level signals (< 5 mV peak-to-peak) of similar magnitude to those expected from the cortex. The impedance of the chip has been measured, and is approximately what is expected from the earlier testing of Chapter IV.

Testing of the chip went on for over 1 week during that time, the chip appeared to function normally. After testing, the chip was allowed to sit for 7 days with a coating of sodium. The chip was then tested again and was no longer functioning. Therefore, a second chip was coated with the silicone rubber and is currently ready for further testing.

VIII. Conclusions and Recommendations

8.1 Current State of the Array

At the beginning of this thesis effort, the AFIT multielctrode array faced several challenges preventing it from being implanted. Through this effort, the majority of these challenges have been met. Provided below is a list of the major challenges and their solutions.

- The array design was modified by removing an on chip clock and adding an 8-bit counter. The counter that has been added is highly reliable and has a fast enough switching speed to allow the array size to be increased to 32 × 32 electrodes.
- The current design requires only 6 I/O connections for 256 electrodes, and the electrode array can be increased in size without increasing the number of connections. This is a significant improvement of the array implanted by Denton and Hensley. Their array required 11 connections and the number of connections increased logarithmically with the number of electrodes.
- The array design was fully simulated. The techniques used for simulation can be modified and used to ensure that future design revisions are correct before they are sent for fabrication.
- Several arrays were fabricated through MOSIS. The returned arrays were fully tested and the electrode's impedance was measured.
- Borrowing from the work of other researchers, a process for coating the electrodes was perfected. This process coats the electrodes using a titanium/iridium bilayer, and the results can be repeated.
- A process for applying polyimide coatings to the array was perfected. This process is repeatable and allows fabricated arrays to be coated in under 1 week of processing.

- A new implantable package has been designed. The new package allows chronic insertion and removal of the array, greatly increasing the flexibility during experimentation. This package is smaller than all previous designs, and can be reliably connected to the AFIT array.
- An encapsulated array has been tested in a saline environment and found to be properly functioning. Signals of the similar potentials to the levels expected on the cortex have been measured. Testing has shown that the array should be expected to function for over 24 hours *in vivo*.

The array can now be ready for implant within one month. During this month it will be necessary to encapsulate several arrays using the methods perfected in this thesis. Further, the implantable package will need to be fabricated with the modifications detailed in Chapter 6. Finally, it will be necessary to find a system for recording the output from the brain chip. However, commercial D/A systems capable of real time storage are available. Further, it is possible to use analog recording systems.

8.2 Recommendations

8.2.1 Recording Systems. Several commercial systems exist that are capable of real time digitization and recording of an input system. The best solution would allow for interface with a standard workstation such as a Sun or NeXT. By initially digitizing the signal, it can be immediately filtered and analyzed.

8.2.2 Implantation. The goal of this thesis was to bring the AFIT array to a point where a second implant was possible, and if time permitted to implant the array. Time has prevented the implantation, but the array is ready to go. This array has great potential for studying the neocortex. Therefore, implantation of the array should be the short term focus of any further work.

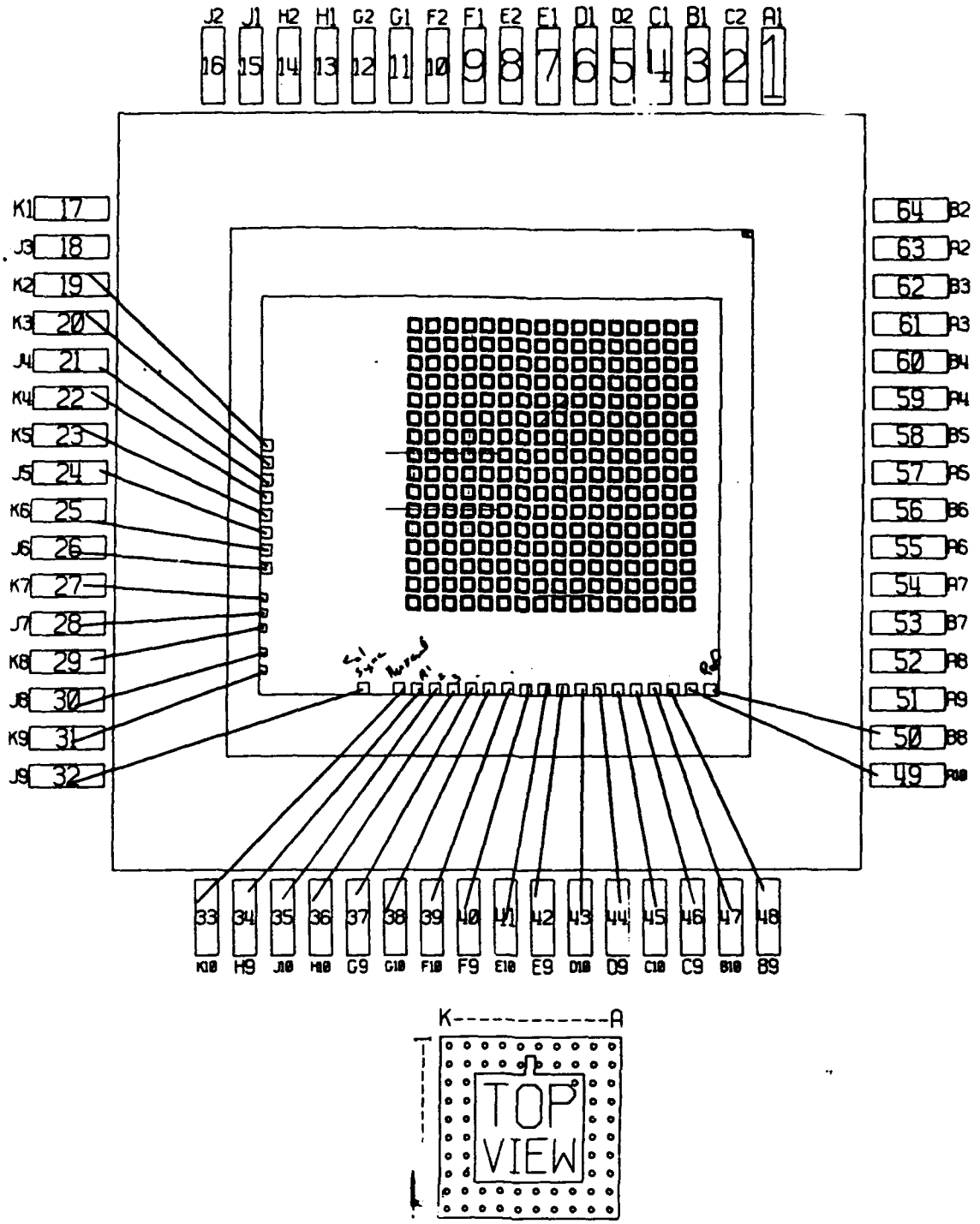
8.2.3 Array Design. As the goal of this thesis was to get a chip ready for implantation, little effort was made to improve the design of the array. The most

pressing improvement needed is the addition of on chip signal amplification. Such amplification will reduce the effect noise has on the signal as it propagates from the chip to the external electronics. Further, on chip amplification could eliminate the need for an external amplifier, thus further simplifying the external electronics.

Another addition that could be of extreme value is the addition of on chip analog to digital (A/D) converters. An on chip A/D converter would decrease the need for external circuitry even further. In fact, direct interface from the chip to a standard port of any digital computer could be achieved. This would greatly aid future experimentations.

Another design change of extreme value would be to further increase the size of the array. An array size of 32×32 could further increase the resolution of the AFIT array, allowing clear definition of individual cortical columns. This would increase the experimental flexibility of the array, and thus increase its value as a research tool.

Appendix A. 64 Pin PGA package bonding diagram



Appendix B. Standard Clean

1. Mechanically agitate chips in an acetone bath for 30 seconds.
2. Immerse chips in an ultrasonic bath of methanol for 1 minute.
3. Blow chips dry with N_2.
4. Bake chips at 200° C for 1 hour.

Appendix C. Metalization Process

1. Clean with standard clean process.
2. Remove from oven and allow to cool.
3. Blow chips with N_2 to remove surface dust.
4. Apply adhesion promoter (HMDS)
   - Puddle HMDS onto the chip. Allow it to spread over the entire chip and coat the edges.
   - Allow to sit for 5 seconds to ensure good coverage of the chip.
   - Spin at 5000 RPM for 45 seconds.
5. Apply positive photo-resist (Shipley AZ1350J)
   - Puddle AZ1350J onto the chip. Allow it to spread over the entire chip and coat the edges.
   - Allow to sit for 5 seconds to ensure good coverage of the chip.
   - Spin at 5000 RPM for 45 seconds.
6. Pre-bake at 70° C for 20 minutes.
7. Align/Expose for 60-65 seconds.
8. Immerse in chlorobenzene for 2 minutes.
9. Bake at 90° C for 15 minutes.
10. Develop photo-resist.
    - Spin at 1000 RPM
    - Spray with AZ351:DIW 1:3 for 45 seconds.
    - Spray with DIW for 30 seconds.
    - Spin dry at 5000 RPM for 45 seconds.

11. Examine pattern. If further develop is neccessary, develop for an addition time.

12. Post-Bake at 90° C for 15 minutes.

13. Sputter Ti for 20 minutes with forward power of 200 W (Approx. 300 microns).

14. Sputter Ir for 75 minutes with forward power of 150 W (Approx. 3000 microns).

15. Immerse in acetone bath. Lightly scrub with a cotton swab to ensure all undesired metal is lifted off of the chip.

Appendix D. Polyimide Application Process

1. Clean chips with the standard clean process.

3. Remove from oven and allow to cool.

4. Blow with N_2 - removes surface dust

5. Apply adhesion promoter (VM-651): (Note the VM-651 must be mixed in a solution of 190 ml methanol, 10 ml DIW, and 1 drop of VM-651, at least 12 hours prior to use. The mixed solution should not be used after 20 days.)

   - Puddle VM-651 onto the chip. Allow it to spread over the entire chip and coat the edges.
   - Allow to sit for 5 seconds to ensure good coverage of the chip.
   - Spin at 5000 RPM for 45 seconds.

6. Apply polyimide (PI-2555):

   - Puddle PI-2555 onto the chip so that it flows over all edges.
   - Allow to sit for 5 seconds to ensure good coverage of the chip.
   - Spin at 4000 RPM for 45 second (Approx. 25 kÅ).

7. Pre-bake at 70° C for 15 minutes. - Dries the polyimide without curing.

8. Remove from oven and allow to cool.

9. Apply negative photo-resist (Waycoat HR-200):

   - Puddle onto the chip allowing it to cover entire chip and sides.
   - Spin at 5000 RPM for 45 seconds.

10. Pre-bake photo-resist at 70° C for 25 minuts.

11. Remove from oven and allow chips to cool.

12. Blow clean with N_2

13. Align/Expose for 4.5 minutes.

14. Develop photo-resist:

    - Spin at 1000 RPM
    - While spinning spray with Xylene for 30 seconds.
    - Spray with butyl acetate for 30 seconds.
    - Spin dry at 5000 RPM for 30 seconds.

15. Examine pattern. If the pattern is not good, then polyimide and photo-resist must be stripped and the process repeated.

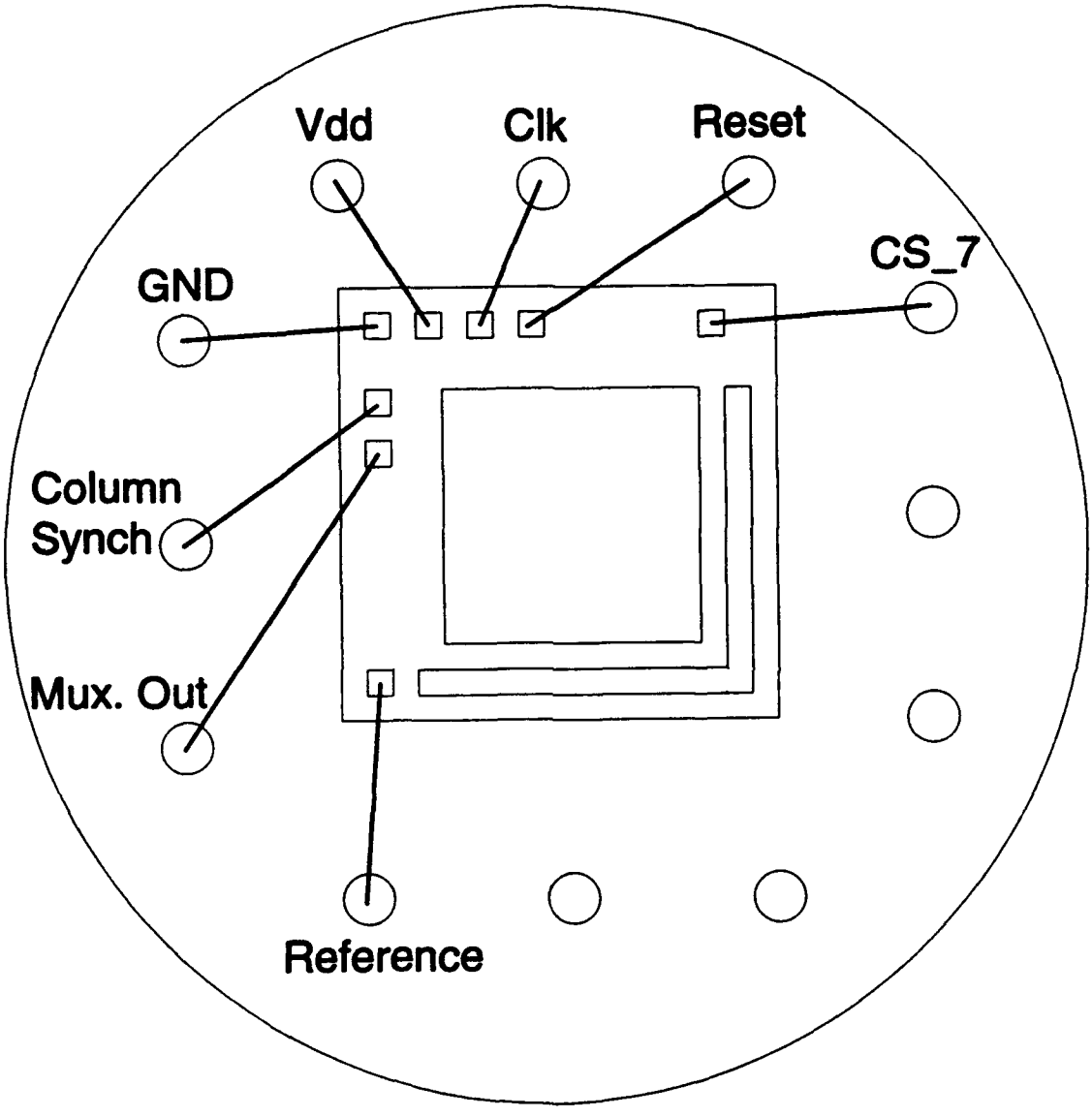
16. Etch the polyimide.

    - Spin at 1000 RPM
    - Spray with AZ351:DIW (1:5) for 3.5-7 seconds depending on which coating this is.
    - Spray with DIW for 30 seconds.
    - Spin dry at 5000 RPM for 30 seconds.

17. Examine to ensure the etch is complete. Etch for additional time if it is required.

18. Final cure at 180° C for 4 hours. Complete cure of the polyimide.

Appendix E. Implantable package bonding diagram



Bibliography

1. Akin, Tayfun and Khalil Najafi. "A Micromachined Silicon Sieve Electrode for Nerve Regeneration Applications." *Proceedings of the 6th. International Conference on Solid-State Sensors and Actuators*. 128–131. 1991.
2. Anderson, David J., et al. "Batch-Fabricated Thin-Film Electrodes for Stimulation of the Central Auditory System," *IEEE Transactions on Biomedical Engineering*, *36*(7):693–703 (July 1989).
3. Ballantine, Robert B. *The Development and Fabrication of an Implantable, Multiplexed, Semiconductor Multielectrode Array*. MS thesis, Air Force Institute of Technology, 1983.
4. Boppart, S.A., et al. "A Flexible Perforated Microelectrode Array for Extended Neural Recordings," *IEEE Transactions on Biomedical Engineering*, *39*(1):37–42 (January 1992).
5. Churchland, Patricia S. and Terrence J. Sejnowski. *The Computational Brain*. The MIT Press, 1992.
6. DeMott, Donald W. "Cortical Micro-toposcopy," *Medical Research Enginee*, *58*(6):1187–1211 (December 1987).
7. DuPont Electronics, Garley Mill Plaza, P.O. Box 80019, Wilmington, DE 19880-0019. *Pyralin Polyimide Coatings*, 1993.
8. Fitzgerald, Gary H. *The Development of a Two-Dimensional Multielectrode Array for Visual Perception Research in the Mammalian Brain*. MS thesis, Air Force Institute of Technology, 1980.
9. German, George W. *A Cortically Implantable Multielectrode Array for Investigating the Mammalian Visual System*. MS thesis, Air Force Institute of Technology, 1981.
10. Guyton, Arthur C. *Textbook of Medical Physiology*. Harcourt Brace Jovanovich, Inc., 1991.
11. Hambrecht. "Phosphenes for visual prosthesis," *NINDS*, *160*:406–454 (1988).
12. Hambrecht, F. T., et al. "Feasibility of an Intracortical Visual Prosthesis for the Blind, I-IV." *Society for Neuroscience*. 1992.
13. Hensley, Russell W. and David C. Denton. *The First Cortical Implant of a Semiconductor Multielectrode Array: Electrode Development and Data Collection*. MS thesis, Air Force Institute of Technology, 1982.
14. Hoogerwerf, A. C. and K. D. Wise. "A Micromachined Silicon Sieve Electrode for Nerve Regeneration Applications." *Proceedings of the 6th. International Conference on Solid-State Sensors and Actuators*. 120–123. 1991.

15. Hubel, D. H. and T. N. Wiesel. "Receptive Fields, Binocular Interaction and Functional Architecture in the Cat's Visual Cortex," *Journal of Physiology*, *160*:406–454 (1962).

16. Jones, Judson P. and Larry A. Palmer. "The Two-Dimensional Spatial Structure of Simple Receptive Fields in Cat Striate Cortex," *Journal of Neurophysiology*, *58*(6):1187–1211 (December 1987).

17. Jones, Judson P., et al. "The Two-Dimensional Spectral Structure of Simple Receptive Fields in Cat Striate Cortex," *Journal of Neurophysiology*, *58*(6):1187–1211 (December 1987).

18. Kabrisky, M., "Personal Correspondance."

19. Kabrisky, Mathew. *A Proposed Model for Visual Information Processing in the Human Brain*. PhD dissertation, University of Illinois, 1966.

20. Kabrisky, Mathew, et al. "A Multiplexed Multi-Electrode Semiconductor Brain Electrode Implant," *IEEE First Annual Conference on Neural Networks*, *39*(9):III–227 to III–242 (June 1987).

21. Kovacs, Gregory T. A. "Regeneration Microelectrode Arrays for Direct Interface to Nerves." *Proceedings of the 6th. International Conference on Solid-State Sensors and Actuators*. 116–119. 1991.

22. Kovacs, Gregory T. A., et al. "Regeneration Microelectrode Array for Peripheral Nerve Recording and Stimulation," *IEEE Transactions on Biomedical Engineering*, *39*(9):893–902 (September 1992).

23. La Voie, Jayme E. *Characterization of a Polyimide for Use as an Inter-metal Insulation*. MS thesis, Air Force Institute of Technology, 1983.

24. LeFevre, Piere K. *Design and Fabrication of an Implantable Cortical Semiconductor Integrated Circuit Electrode Array*. MS thesis, Air Force Institute of Technology, 1990.

25. Niedermeyer, Ernst and Fernando Lopes da Silva. *Electroencephalography, Basic Principles, Clinical Applications, and Related Fields*. Urban and Schwarzenberg, 1982.

26. Szczublewski, David P. *The Redesign of a Multielectrode Semiconductor Array Intended for Implantation into the Brain of a Rhesus Monkey*. MS thesis, Air Force Institute of Technology, 1989.

27. Sze, S. M. *Semiconductor Devices: Physics and Technology*. John Wiley and Sons, 1981.

28. Tatman, Joseph A. *A Two-Dimensional Multielectrode Microprobe for the Visual Cortex*. MS thesis, Air Force Institute of Technology, 1979.

29. Tootell, Roger B. H., et al. "Deoxyglucose Analysis of Retinopic Organization in Primate Striate Cortex," *Science*, *218*(26):902–904 (November 1982).

30. Turner, Ricardo R. *Encapsulation and Packaging of a Semiconductor Multi-electrode Array for Cortical Implantation*. MS thesis, Air Force Institute of Technology, 1984.

31. Wise, Kensall D. and Khalil Najafi. "A Micromachined Integrated Sensor with On-Chip Self-Test Capability." *IEEE Transducers, International Conference on Solid State Sensors and Actuators - Digest of Technical Papers*. 12–16. 1984.

32. Ziaie, Babak, et al. "A High-Current $IrOx$ Thin-Film Neuromuscular Microstimulator." *Proceedings of the 6th. International Conference on Solid-State Sensors and Actuators*. 124–127. 1991.

Vita

Lt. Reid was born in Okinawa Japan on 17 April 1970 to James R. and Penelope A. Reid. He graduated from Keystone School in San Antonio, Texas in 1988. He was then fortunate enough to attend Duke University on a ROTC scholorship, graduating in May 1992 with a B.S. in electrical engineering. After being commissioned a second lieutenant in the U.S. Air Force, he was assigned to the Air Force Institute of Technology to pursue a Masters degree in electrical engineering.

Permanent address: 1014 Courtney Dr.
Dayton, Ohio 45431

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	December 1993	Master's Thesis

4. TITLE AND SUBTITLE
The AFIT Multielectrode Array for Neural Recording and Stimulation: Design, Testing, and Encapsulation

5. FUNDING NUMBERS

6. AUTHOR(S)
James R. Reid, Jr.

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Air Force Institute of Technology, WPAFB OH 45433-7765

8. PERFORMING ORGANIZATION REPORT NUMBER
AFIT/GE/ENG/93D-33

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Mr. Ed Zelnio
WL/AARA
WPAFB, OH 45433

10. SPONSORING / MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION / AVAILABILITY STATEMENT
Approved for public release; distribution unlimited

12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words)*

A two-dimensional, X-Y addressable, multiplexed array of 256 electrodes (16 x 16) has been fabricated using conventional semiconductor processing techniques. The individual electrodes are $160\mu m \times 160\mu m$, approximating the size of the cortical columns; the overall array size is $3910\mu m \times 3910\mu m$. The array has been fitted to a chronically implantable package and tested for several days in a simulated neural environment. EEG-like data were collected successfully from individual electrodes in the array. This array improves on a previous design of a 16 electrode (4 x 4) array that was chronically implanted on the cortex of a laboratory beagle (Canis familiaris) in 1982. The original implant, located approximately over primary visual cortex, recorded both EEG and visually evoked response (VER) data. It proved the feasibility of multiplexing data directly from the surface of the cortex, thereby opening the possibility of very large arrays of electrodes since only a single wideband signal channel could address significant numbers of electrodes.

14. SUBJECT TERMS	15. NUMBER OF PAGES
Neural electrodes, Brain, EEG	104
	16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	UL